

# WCDMA/HSPA Scenario Version (3)

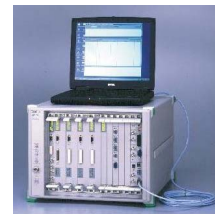
**MD8480C**

W-CDMA Signalling Tester

# Details of HSDPA C–Scenario

How to Use Scenario Library and Structure for HSDPA

Version 1.0  
Anritsu Corporation



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MD8480C-E-E-4

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DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps  
SRBs for DCCH)

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# Radio Bearer for HSDPA Configuration

```

/* Origination arrow diagram in this Scenario */
/* MS MD8480 */
/* |----- RRC Connection Request ---->| */
/* | (TR-Mode PRACH-RACH-CCCH) | */
/* |<----- RRC Connection Setup ---->| */
/* | (UM-Mode S-CCPCH-FACH-CCCH) | */
/* |----- RRC Connection Setup Complete ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |----- MM CM Service Request ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |<----- GMM AuthenticAndCiphering Req. ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |----- GMM AuthenticAndCiphering Resp.---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |<----- Security Mode Command ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |----- Security Mode Complete ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |----- SM Activate PDP Context Request ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |<----- Radio Bearer Setup ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* ===== HS & Associated DPCH Configuration ===== */
/* |----- Radio Bearer Setup Complete ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */
/* |<----- SM Activate PDP Context Accept ---->| */
/* | (AM-Mode DPCH-DCH-DCCH) | */

```

```

INT CFN; /* Cell Frame Number */
CFN = ((BitsReadCFN(UNIT_BTS1, NO_TIMEOUT) + 150) % 256) & (short)( ~(4-1) );

/* Send Message: Radio Bearer Setup */
UCHAR SndData[] = { /* This "Radio Bearer Setup" message should match to the HSDPA configuration on the BTS */ };
RlcMUI = 1;
RlcCNF = 1;
SndMessageIntegrity( UNIT_BTS1, RLC_AM_DATA_REQ, D_DCCH, 1, SndData, 743 );
RlcCNF = 0;

CalcRMParameter( D_DPCH, &CphyRISetup_D_DPCH_HSDPA, &CphyTrchConfig_D_DPCH_HSDPA );
CphyRISetup( UNIT_BTS1, D_DPCH, 0, &CphyRISetup_D_DPCH_HSDPA, CFN, ... );
CphyTrchConfig( UNIT_BTS1, D_DPCH, 0, &CphyTrchConfig_D_DPCH_HSDPA, CFN, ... );
CmacConfig( UNIT_BTS1, D_DPCH, 0, &CmacConfig_D_DPCH_HSDPA, CFN, ... );

CalcRMParameter( U_DPCH, &CphyRISetup_U_DPCH_HSDPA, &CphyTrchConfig_U_DPCH_HSDPA );
CphyRISetup( UNIT_BTS1, U_DPCH, 0, &CphyRISetup_U_DPCH_HSDPA, CFN, ... );
CphyTrchConfig( UNIT_BTS1, U_DPCH, 0, &CphyTrchConfig_U_DPCH_HSDPA, CFN, ... );
CmacConfig( UNIT_BTS1, U_DPCH, 0, &CmacConfig_U_DPCH_HSDPA, CFN, ... );

CrlcConfig( UNIT_BTS1, CRLC_AM_ESTABLISH, DTCH, 0, &Packet_CrlcConfig_DTCH, TE, ... );

CphyHsSetup( UNIT_BTS1, D_HS_SCCH, 0, &CphyHsSetupHS_SCCH_C12, CFN, ... );
CphyHsSetup( UNIT_BTS1, D_HS_PDSCH, 0, &CphyHsSetupHS_PDSCH_C12, CFN, ... );
CphyHsSetup( UNIT_BTS1, U_HS_DPCCH, 0, &CphyHsSetupHS_DPCCH_C12, CFN, ... );
CmacHsConfig( UNIT_BTS1, HSDSCH, 0, &CmacHsConfigHS_DSCH_C12, CFN, ... );

/* Receive Message: Radio Bearer Setup Complete */
ret = RcvMessageIntegrity( &BitsNo, &Frame, &Lo_Ch, &Lo_No, RcvData, ... );
...if ( GetMessageTypeId( U_DCCH, RcvData ) == Dec2005R5_RadioBearerSetupComplete ) ...

```

# Structure Setting for Associated DPCH

TS34.108 6.10.2.4.5.2 Interactive or background/UL: 384 DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH

For Uplink, refer to:

TS34.108 6.10.2.4.1.34 Interactive or Background/UL: 384 DL: 384 kbps/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH

Uplink DPCH-Layer 1  
Uplink DPCH-MAC, RLC

For Downlink, refer to:

TS34.108 6.10.2.4.1.2 Stand-alone UL: 3.4 DL: 3.4 kbps SRBs for DCCH

Downlink DPCH-Layer 1  
Downlink DPCH-MAC, RLC

## Uplink DPCH—Layer 1 (TS34.108 6.10.2.4.1.34 Interactive or Background/UL: 384 DL: 384 kbps/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

DPCH Uplink	Min spreading factor	4			
	Max number of DPCH data bits/radio frame	9 600			
	Number of DPDCH	1			
	Puncturing Limit	0.64			
TFCS size		18 (alt 12)			
TFCS	(384 kbps RAB, DCCH)= (TF0, TF0), (TF1, TF0), (TF2, TF0), (TF3, TF0), (TF4, TF0), (TF5, TF0), (TF6, TF0), (TF7, TF0), (TF8, TF0), (TF6, TF1), (TF7, TF1), (TF8, TF1) (alt (TF0, TF0), (TF1, TF0), (TF2, TF0), (TF3, TF0), (TF4, TF0), (TF5, TF0), (TF0, TF1), (TF1, TF1), (TF2, TF1), (TF3, TF1), (TF4, TF1), (TF5, TF1))				
Higher layer	RAB/signalling RB	SRB#1	SRB#2	SRB#3	SRB#4
	User of Radio Bearer	RRC	RRC	NAS_DT High prio	NAS_DT Low prio
RLC	Logical channel type	DCCH	DCCH	DCCH	DCCH
	RLC mode	UM	AM	AM	AM
	Payload sizes, bit	136	128	128	128
	Max data rate, bps	3 400	3 200	3 200	3 200
	AMD/UMD PDU header, bit	8	16	16	16
MAC	MAC header, bit	4	4	4	4
	MAC multiplexing	4 logical channel multiplexing			
Layer 1	TrCH type	DCH			
	TB sizes, bit	148 (alt 0, 148)			
	TFS	TF0, bits	0x148 (alt 1x0)		
		TF1, bits	1x148		
	TTI, ms	40			
	Coding type	CC 1/3			
	CRC, bit	16			
	Max number of bits/TTI before rate matching	516			
	Uplink: Max number of bits/radio frame before rate matching	129			
	RM attribute	155 to 185			

```

CphyRlSetupPar = &CphyRlSetup_U_DPCH_HSDPA;
memset(CphyRlSetupPar, 0, sizeof(CPHY_RL_SETUP_PAR));
CphyRlSetupPar->ScsCode = SC17;
CphyRlSetupPar->ScsCode = SC1000000;
CphyRlSetupPar->Format = DCCH_FORMAT;
CphyRlSetupPar->SymbolRate = SWRAT960K; /* for DPCH */
CphyRlSetupPar->NumOfDPDCH = 1;
CphyRlSetupPar->DchCode = DIVERSITY_OFF;
CphyRlSetupPar->TxDiversity = DIVERSITY_OFF;

CphyTrchConfigPar = &CphyTrchConfig_U_DPCH_HSDPA;
memset(CphyTrchConfigPar, 0, sizeof(CPHY_TRCH_CONFIG_PAR));
CphyTrchConfigPar->DPXPosition = INTERLEAVE_ON;
CphyTrchConfigPar->InterleaveMod = INTERLEAVE_ON;
CphyTrchConfigPar->PunctLimit = 64;

CphyTrchConfigPar->TFCS.NumOfTFCS = 12;

CphyTrchConfigPar->TFCS.TFCS[0][0] = 0; /* DCH #0 */
CphyTrchConfigPar->TFCS.TFCS[0][1] = 0; /* DCH #1 */
CphyTrchConfigPar->TFCS.TFCS[1][0] = 1; /* DCH #2 */
CphyTrchConfigPar->TFCS.TFCS[1][1] = 0; /* DCH #3 */
CphyTrchConfigPar->TFCS.TFCS[2][0] = 2; /* DCH #4 */
CphyTrchConfigPar->TFCS.TFCS[2][1] = 0; /* DCH #5 */
CphyTrchConfigPar->TFCS.TFCS[3][0] = 3; /* DCH #6 */
CphyTrchConfigPar->TFCS.TFCS[3][1] = 0; /* DCH #7 */
CphyTrchConfigPar->TFCS.TFCS[4][0] = 4; /* DCH #8 */
CphyTrchConfigPar->TFCS.TFCS[4][1] = 0; /* DCH #9 */
CphyTrchConfigPar->TFCS.TFCS[5][0] = 5; /* DCH #10 */
CphyTrchConfigPar->TFCS.TFCS[5][1] = 0; /* DCH #11 */
CphyTrchConfigPar->TFCS.TFCS[6][0] = 0; /* DCH #12 */
CphyTrchConfigPar->TFCS.TFCS[6][1] = 0; /* DCH #13 */
CphyTrchConfigPar->TFCS.TFCS[7][0] = 1; /* DCH #14 */
CphyTrchConfigPar->TFCS.TFCS[7][1] = 0; /* DCH #15 */
CphyTrchConfigPar->TFCS.TFCS[8][0] = 2; /* DCH #16 */
CphyTrchConfigPar->TFCS.TFCS[8][1] = 0; /* DCH #17 */
CphyTrchConfigPar->TFCS.TFCS[9][0] = 3; /* DCH #18 */
CphyTrchConfigPar->TFCS.TFCS[9][1] = 0; /* DCH #19 */
CphyTrchConfigPar->TFCS.TFCS[10][0] = 4; /* DCH #20 */
CphyTrchConfigPar->TFCS.TFCS[10][1] = 0; /* DCH #21 */
CphyTrchConfigPar->TFCS.TFCS[11][0] = 5; /* DCH #22 */
CphyTrchConfigPar->TFCS.TFCS[11][1] = 0; /* DCH #23 */
CphyTrchConfigPar->NumOfTrch = 2;

CphyTrchConfigPar->TrchInfo[0].Trch = U_DCH;
CphyTrchConfigPar->TrchInfo[0].TrchNo = 07;
CphyTrchConfigPar->TrchInfo[0].InterleaveMod = INTERLEAVE_ON;
CphyTrchConfigPar->TrchInfo[0].Static_TTI = 1;
CphyTrchConfigPar->TrchInfo[0].Static_SFType = CODING_TURBO;
CphyTrchConfigPar->TrchInfo[0].Static_CodingRate = CODINGRATE1_3;
CphyTrchConfigPar->TrchInfo[0].Static_CRC_Size = 16;
CphyTrchConfigPar->TrchInfo[0].Static_RM_Attr = 110;
CphyTrchConfigPar->TrchInfo[0].NumOfDynamic = 6;
CphyTrchConfigPar->TrchInfo[0].Dynamic[0].NumOfTBs = 0;
CphyTrchConfigPar->TrchInfo[0].Dynamic[0].TBSsize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[1].NumOfTBs = 1;
CphyTrchConfigPar->TrchInfo[0].Dynamic[1].TBSsize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[2].NumOfTBs = 2;
CphyTrchConfigPar->TrchInfo[0].Dynamic[2].TBSsize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[3].NumOfTBs = 4;
CphyTrchConfigPar->TrchInfo[0].Dynamic[3].TBSsize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[4].NumOfTBs = 8;
CphyTrchConfigPar->TrchInfo[0].Dynamic[4].TBSsize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[5].NumOfTBs = 12;
CphyTrchConfigPar->TrchInfo[0].Dynamic[5].TBSsize = 336;
CphyTrchConfigPar->TrchInfo[5].TBSsize = 336;

CphyTrchConfigPar->TrchInfo[1].Trch = U_DCH;
CphyTrchConfigPar->TrchInfo[1].TrchNo = 17;
CphyTrchConfigPar->TrchInfo[1].InterleaveMod = INTERLEAVE_ON;
CphyTrchConfigPar->TrchInfo[1].Static_TTI = 4;
CphyTrchConfigPar->TrchInfo[1].Static_SFType = CODING_CONV;
CphyTrchConfigPar->TrchInfo[1].Static_CodingRate = CODINGRATE1_3;
CphyTrchConfigPar->TrchInfo[1].Static_CRC_Size = 16;
CphyTrchConfigPar->TrchInfo[1].Static_RM_Attr = 160;
CphyTrchConfigPar->TrchInfo[1].NumOfDynamic = 2;
CphyTrchConfigPar->TrchInfo[1].Dynamic[0].NumOfTBs = 0;
CphyTrchConfigPar->TrchInfo[1].Dynamic[0].TBSsize = 148;
CphyTrchConfigPar->TrchInfo[1].Dynamic[1].NumOfTBs = 1;
CphyTrchConfigPar->TrchInfo[1].Dynamic[1].TBSsize = 148;
    
```

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## Uplink DPCH—MAC, RLC (TS34.108 6.10.2.4.1.34 Interactive or Background/UL:384 DL: 384 kbps/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

Higher layer	RAB/signalling RB	SRB#1	SRB#2	SRB#3	SRB#4
	User of Radio Bearer	RRC	RRC	NAS_DT High prio	NAS_DT Low prio
RLC	Logical channel type	DCCH	DCCH	DCCH	DCCH
	RLC mode	UM	AM	AM	AM
	Payload sizes, bit	136	128	128	128
	Max data rate, bps	3 400	3 200	3 200	3 200
	AMD/UMD PDU header, bit	8	16	16	16
MAC	MAC header, bit	4	4	4	4
	MAC multiplexing	4 logical channel multiplexing			
Layer 1	TrCH type	DCH			
	TB sizes, bit	148 (alt 0, 148)			
	TFS	TF0, bits	0x148 (alt 1x0)		
		TF1, bits	1x148		
	TTI, ms	40			
	Coding type	CC 1/3			
	CRC, bit	16			
	Max number of bits/TTI before rate matching	516			
	Uplink: Max number of bits/radio frame before rate matching	129			
	RM attribute	155 to 185			

```

CrlcConfigPar = &CrlcConfig_DCCH;
memset(CrlcConfigPar, 0, sizeof(CRLC_CONFIG_PAR));
CrlcConfigPar->NumOfPUS = 1;
CrlcConfigPar->PU_LengthTM = 0;
CrlcConfigPar->PU_LengthUM = 136;
CrlcConfigPar->PU_LengthAM = 128;

CmacConfigPar = &CmacConfig_U_DPCH_HSDPA;
memset(CmacConfigPar, 0, sizeof(CMAC_CONFIG_PAR));
CmacConfigPar->MAC_Active = MAC_ACTIVE;

CmacConfigPar->NumOfLoch[0] = 1;
CmacConfigPar->LochInfo[0][0].Loch = U_DCH;
CmacConfigPar->LochInfo[0][0].LochNo = 07;
CmacConfigPar->LochInfo[0][0].Priority = 0;
CmacConfigPar->LochInfo[0][0].CTLength = 0;
CmacConfigPar->LochInfo[0][0].CTValue = 0;
CmacConfigPar->LochInfo[0][0].RCPLength = 0;
CmacConfigPar->LochInfo[0][0].URType = URID_NOTUSE;
CmacConfigPar->LochInfo[0][0].URID = 0;

CmacConfigPar->NumOfLoch[1] = 4;
CmacConfigPar->LochInfo[1][0].Loch = U_DCH;
CmacConfigPar->LochInfo[1][0].LochNo = 07;
CmacConfigPar->LochInfo[1][0].Priority = 0;
CmacConfigPar->LochInfo[1][0].CTLength = 0;
CmacConfigPar->LochInfo[1][0].CTValue = 0;
CmacConfigPar->LochInfo[1][0].RCPLength = 0;
CmacConfigPar->LochInfo[1][0].URType = URID_NOTUSE;
CmacConfigPar->LochInfo[1][0].URID = 0;
CmacConfigPar->LochInfo[1][1].Loch = U_DCH;
CmacConfigPar->LochInfo[1][1].LochNo = 17;
CmacConfigPar->LochInfo[1][1].Priority = 4;
CmacConfigPar->LochInfo[1][1].CTLength = 0;
CmacConfigPar->LochInfo[1][1].CTValue = 0;
CmacConfigPar->LochInfo[1][1].RCPLength = 0;
CmacConfigPar->LochInfo[1][1].URType = URID_NOTUSE;
CmacConfigPar->LochInfo[1][1].URID = 0;
CmacConfigPar->LochInfo[1][2].Loch = U_DCH;
CmacConfigPar->LochInfo[1][2].LochNo = 07;
CmacConfigPar->LochInfo[1][2].Priority = 0;
CmacConfigPar->LochInfo[1][2].CTLength = 0;
CmacConfigPar->LochInfo[1][2].CTValue = 0;
CmacConfigPar->LochInfo[1][2].RCPLength = 0;
CmacConfigPar->LochInfo[1][2].URType = URID_NOTUSE;
CmacConfigPar->LochInfo[1][2].URID = 0;
CmacConfigPar->LochInfo[1][3].Loch = U_DCH;
CmacConfigPar->LochInfo[1][3].LochNo = 37;
CmacConfigPar->LochInfo[1][3].Priority = 4;
CmacConfigPar->LochInfo[1][3].CTLength = 0;
CmacConfigPar->LochInfo[1][3].CTValue = 0;
CmacConfigPar->LochInfo[1][3].RCPLength = 0;
CmacConfigPar->LochInfo[1][3].URType = URID_NOTUSE;
CmacConfigPar->LochInfo[1][3].URID = 0;
    
```

TS23.321-Table 9.2.1.5a: Structure of the C/T field

C/T field	Designation
0000	Logical channel 1
0001	Logical channel 2
...	...
1110	Logical channel 15
1111	Reserved

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## Uplink DPCH—Layer 1, MAC, RLC Traffic CH (TS34.108 6.10.2.4.1.34 Interactive or Background/UL: 384 DL: 384 kbps/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

Higher layer	RAB/Signalling RB	RAB	
RLC	Logical channel type	DTCH	
	RLC mode	AM	
	Payload sizes, bit	320	
	Max data rate, bps	384 000	
MAC	MAC header, bit	0	
	MAC multiplexing	N/A	
Layer 1	TrCH type	DCH	
	TF sizes, bit	336	
	TFS	TF0, bits	0x336
		TF1, bits	1x336
		TF2, bits	2x336
		TF3, bits	4x336
		TF4, bits	8x336
		TF5, bits	12x336
		TF6, bits	16x336(alt. N/A)
		TF7, bits	20x336(alt. N/A)
	TF8, bits	24x336 (alt. N/A)	
	TTI, ms	20 (alt. 10)	
	Coding type	TC	
CRC, bit	16		
Max number of bits/TTI after channel coding	25 368		
Uplink: Max number of bits/radio frame before rate matching	12 684		
RM attribute	110-180		

```

CrlicConfigPar = sPacket_CrlicConfig_DPCH;
memset( crlicConfigPar, 0, sizeof( CrlicConfigPar ) );
CrlicConfigPar->NumOfTFs    = 14;
CrlicConfigPar->FU_LengthTM  = 244;
CrlicConfigPar->FU_LengthUM  = 328;
CrlicConfigPar->FU_LengthAM  = 320;

CphyTrchConfigPar->TrchInfo[0].Trch      = U_DCH;
CphyTrchConfigPar->TrchInfo[0].TrchNo   = 0;
CphyTrchConfigPar->TrchInfo[0].InterLev = INTERLEAVE_ON;

CphyTrchConfigPar->TrchInfo[0].Static.TTI      = 1;
CphyTrchConfigPar->TrchInfo[0].Static.EPType   = CODING_TURBO;
CphyTrchConfigPar->TrchInfo[0].Static.CodingRate = CODINGRATE_3;
CphyTrchConfigPar->TrchInfo[0].Static.CRC_Size = 16;
CphyTrchConfigPar->TrchInfo[0].Static.RM_Attr  = 110;

CphyTrchConfigPar->TrchInfo[0].NumOfDynamic = 6;
CphyTrchConfigPar->TrchInfo[0].Dynamic[0].NumOfTB = 0;
CphyTrchConfigPar->TrchInfo[0].Dynamic[0].TBSize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[1].NumOfTB = 1;
CphyTrchConfigPar->TrchInfo[0].Dynamic[1].TBSize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[2].NumOfTB = 2;
CphyTrchConfigPar->TrchInfo[0].Dynamic[2].TBSize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[3].NumOfTB = 4;
CphyTrchConfigPar->TrchInfo[0].Dynamic[3].TBSize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[4].NumOfTB = 8;
CphyTrchConfigPar->TrchInfo[0].Dynamic[4].TBSize = 336;
CphyTrchConfigPar->TrchInfo[0].Dynamic[5].NumOfTB = 12;
CphyTrchConfigPar->TrchInfo[0].Dynamic[5].TBSize = 336;

CmacConfigPar->NumOfLoch[0] = 1;
CmacConfigPar->LochInfo[0][0].LochNo = 0;
CmacConfigPar->LochInfo[0][0].Priority = 0;
CmacConfigPar->LochInfo[0][0].CTValue = 0;
CmacConfigPar->LochInfo[0][0].TxFLength = 0;
CmacConfigPar->LochInfo[0][0].UEIDType = UEID_NOTUSE;
CmacConfigPar->LochInfo[0][0].UEID = 0;
    
```

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## Downlink DPCH—Layer 1 (TS34.108 6.10.2.4.1.2 Stand-alone UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

DPCH Downlink	DTX position	Fixed				
	Spreading factor	256				
	DPCCCH	Number of TFCI bits/slot	0			
		Number of TPC bits/slot	2			
	DPDCH	Number of Pilot bits/slot	4			
		Number of data bits/slot	14			
	Number of data bits/frame	210				
TFCS size	2					
TFCS	SRBs for DCCH = TF0, TF1					
Higher layer	RAB/signalling RB	SRB#1	SRB#2	SRB#3	SRB#4	
	User of Radio Bearer	RRC	RRC	NAS_DT High prio	NAS_DT Low prio	
RLC	Logical channel type	DCCH	DCCH	DCCH	DCCH	
	RLC mode	UM	AM	AM	AM	
	Payload sizes, bit	136	128	128	128	
	Max data rate, bps	3 400	3 200	3 200	3 200	
	AMDU/MD PDU header, bit	8	16	16	16	
MAC	MAC header, bit	4	4	4	4	
	MAC multiplexing	4 logical channel multiplexing				
Layer 1	TrCH type	DCH				
	TF sizes, bit	148 (alt 0, 148) (note)				
	TFS	TF0, bits	0x148 (alt 1x0) (note)			
		TF1, bits	1x148			
	TTI, ms	40				
	Coding type	CC 1/3				
	CRC, bit	16				
	Max number of bits/TTI before rate matching	516				
RM attribute	155 to 230					
NOTE:	Alternative parameters enable the measurement "transport channel BLER" in the UE.					

```

CphyRlSetupPar = sCphyRlSetup_D_DPCH_HSDPA;
memset( CphyRlSetupPar, 0, sizeof( CPHY_RL_SETUP_PAR ) );
CphyRlSetupPar->ScramCode = 7680;
CphyRlSetupPar->ScramCode = 0x00000090;
CphyRlSetupPar->SymbolRate = SymbRate_4; // for DPCCCH //
CphyRlSetupPar->SlotFormat = SLOT_FORMAT_4; // for DPCCCH //
CphyRlSetupPar->ChCode = 10;
CphyRlSetupPar->NumOfDPCCCH = 1;
CphyRlSetupPar->Power = POWER_STEP_01DB(-143); // Power = -14.3dB //
CphyRlSetupPar->Dpch[0].Power = POWER_STEP_01DB(-143); // Power = -14.3dB //
CphyRlSetupPar->Dpch[0].ChCode = 10;
CphyRlSetupPar->TxDiversity = DIVERSITY_OFF;
CphyRlSetupPar->MaxDLPower = 0;
CphyRlSetupPar->MaxULPower = -99;

CphyTrchConfigPar = sCphyTrchConfig_D_DPCH_HSDPA;
memset( CphyTrchConfigPar, 0, sizeof( CPHY_TRCH_CONFIG_PAR ) );
CphyTrchConfigPar->DTXPosition = DTX_FIXED_POSITION;
CphyTrchConfigPar->InterLev = INTERLEAVE_ON;
CphyTrchConfigPar->NumOfTrch = 1;

CphyTrchConfigPar->TFCS.NumOfTFC = 2;
CphyTrchConfigPar->TFCS.TFC[0][0] = 0; // DCH#0 // TFCI = 0 //
CphyTrchConfigPar->TFCS.TFC[1][0] = 1; // DCH#0 // TFCI = 1 //

CphyTrchConfigPar->TrchInfo[0].Trch      = D_DCH;
CphyTrchConfigPar->TrchInfo[0].TrchNo   = 0;
CphyTrchConfigPar->TrchInfo[0].InterLev = INTERLEAVE_ON;

CphyTrchConfigPar->TrchInfo[0].Static.TTI      = 4;
CphyTrchConfigPar->TrchInfo[0].Static.EPType   = CODING_CONV;
CphyTrchConfigPar->TrchInfo[0].Static.CodingRate = CODINGRATE1_3;
CphyTrchConfigPar->TrchInfo[0].Static.CRC_Size = 16;
CphyTrchConfigPar->TrchInfo[0].Static.RM_Attr  = 160;

CphyTrchConfigPar->TrchInfo[0].NumOfDynamic = 2;
CphyTrchConfigPar->TrchInfo[0].Dynamic[0].NumOfTB = 0;
CphyTrchConfigPar->TrchInfo[0].Dynamic[0].TBSize = 148;
CphyTrchConfigPar->TrchInfo[0].Dynamic[1].NumOfTB = 1;
CphyTrchConfigPar->TrchInfo[0].Dynamic[1].TBSize = 148;
    
```

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## Downlink DPCH-MAC, RLC (TS34.108 6.10.2.4.1.2 Stand-alone UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

Higher layer	RAB/signalling RB	SRB#1	SRB#2	SRB#3	SRB#4	
	User of Radio Bearer	RRC	RRC	NAS_DT High prio	NAS_DT Low prio	
RLC	Logical channel type	DCCH	DCCH	DCCH	DCCH	
	RLC mode	UM	AM	AM	AM	
	Payload sizes, bit	136	128	128	128	
	Max data rate, bps	3 400	3 200	3 200	3 200	
	AMD/UMD PDU header, bit	8	16	16	16	
MAC	MAC header, bit	4	4	4	4	
	MAC multiplexing	4 logical channel multiplexing				
Layer 1	TrCH type	DCH				
	TB sizes, bit	148 (alt 0, 148) (note)				
	TFS	TF0, bits	0x148 (alt 1x0) (note)			
		TF1, bits	1x148			
	TTI, ms	40				
	Coding type	CC 1/3				
	CRC, bit	16				
	Max number of bits/TTI before rate matching	516				
	RM attribute	155 to 230				
	NOTE: Alternative parameters enable the measurement "transport channel BLER" in the UE.					

```

CrIcConfigPar = &CrIcConfig_DCCH;
memset( CrIcConfigPar, 0, sizeof(CRlcConfigPar) );
CrIcConfigPar->NumOfPUS = 1;
CrIcConfigPar->PU_LengthTM = 0;
CrIcConfigPar->PU_LengthUM = 136;
CrIcConfigPar->PU_LengthAM = 128;
    
```

```

CmacConfigPar = &CmacConfig_B_DCCH_SRB3;
memset( CmacConfigPar, 0, sizeof(CMAC_CONFIG_PAR) );
CmacConfigPar->ActFlag = MAC_ACTIVE;

CmacConfigPar->NumOfLoch[0] = 4;
CmacConfigPar->LochInfo[0][0].Loch = D_DCCH;
CmacConfigPar->LochInfo[0][0].LochNo = 0;
CmacConfigPar->LochInfo[0][0].Priority = 0;
CmacConfigPar->LochInfo[0][0].CTLength = 4;
CmacConfigPar->LochInfo[0][0].CTValue = 0;
CmacConfigPar->LochInfo[0][0].NCTLength = 0;
CmacConfigPar->LochInfo[0][0].UEIDType = UEID_NOTUSE;
CmacConfigPar->LochInfo[0][0].UEID = 0;

CmacConfigPar->LochInfo[0][1].Loch = D_DCCH;
CmacConfigPar->LochInfo[0][1].LochNo = 1;
CmacConfigPar->LochInfo[0][1].Priority = 0;
CmacConfigPar->LochInfo[0][1].CTLength = 4;
CmacConfigPar->LochInfo[0][1].CTValue = 0;
CmacConfigPar->LochInfo[0][1].NCTLength = 0;
CmacConfigPar->LochInfo[0][1].UEIDType = UEID_NOTUSE;
CmacConfigPar->LochInfo[0][1].UEID = 0;

CmacConfigPar->LochInfo[0][2].Loch = D_DCCH;
CmacConfigPar->LochInfo[0][2].LochNo = 2;
CmacConfigPar->LochInfo[0][2].Priority = 0;
CmacConfigPar->LochInfo[0][2].CTLength = 4;
CmacConfigPar->LochInfo[0][2].CTValue = 2;
CmacConfigPar->LochInfo[0][2].NCTLength = 0;
CmacConfigPar->LochInfo[0][2].UEIDType = UEID_NOTUSE;
CmacConfigPar->LochInfo[0][2].UEID = 0;

CmacConfigPar->LochInfo[0][3].Loch = D_DCCH;
CmacConfigPar->LochInfo[0][3].LochNo = 3;
CmacConfigPar->LochInfo[0][3].Priority = 0;
CmacConfigPar->LochInfo[0][3].CTLength = 4;
CmacConfigPar->LochInfo[0][3].CTValue = 3;
CmacConfigPar->LochInfo[0][3].NCTLength = 0;
CmacConfigPar->LochInfo[0][3].UEIDType = UEID_NOTUSE;
CmacConfigPar->LochInfo[0][3].UEID = 0;
    
```

TS25.321-Table 9.2.1.5a: Structure of the C/T field

C/T field	Designation
0000	Logical channel 1
0001	Logical channel 2
...	...
1110	Logical channel 15
1111	Reserved

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Anritsu

## TS34.108 6.10.2.4.5.2 Interactive or Background/UL: 384 DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH

### HSDPA Channels

- Downlink HS-SCCH
- Downlink HS-PDSCH
- Downlink HS-DSCH
- Uplink HS-DPCCH

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Anritsu

# HSDPA Channels (TS34.108 6.10.2.4.5.2 Interactive or Background/UL: 384 DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

TS25.306 Table 5.1a: FDD HS-DSCH physical layer categories

HS-DSCH category	Maximum number of HS-DSCH codes received	Minimum inter-TTI interval	Maximum number of bits of HS-DSCH transport block received within HS-DSCH TTI	Total number of soft channel bits
Category 1	3	3	7298	19200
Category 2	5	3	7298	28800
Category 3	5	2	7298	28800
Category 4	5	2	7298	38400
Category 5	5	1	7298	57600
Category 6	5	1	7298	67200
Category 7	10	1	14411	115200
Category 8	10	1	14411	134400
Category 9	15	1	20251	172800
Category 10	15	1	27952	172800
Category 11	5	2	3630	14400
<b>Category 12</b>	<b>5</b>	<b>1</b>	<b>3630</b>	<b>28800</b>
Category 13	15	1	34800	259200
Category 14	15	1	42196	259200
Category 15	15	1	23370	345600
Category 16	15	1	27952	345600

Higher layer	RAB/Signalling RB	RAB
RLC	Logical channel type	DTCH
	RLC mode	AM
	Payload sizes, bit	320 (alt. 640)
	Max data rate, bps	depends on UE category
	AMD PDU header, bit	NOTE1 16
MAC	MAC-d header, bit	0
	MAC multiplexing	N/A
	MAC-d PDU size, bit	<b>336</b> (alt. 656)
	MAC-hs header fixed part, bit	21
Layer 1	TrCH type	HS-DSCH
	TTI	2 ms
	Coding type	TC
	CRC, bit	24

NOTE: The peak throughput may be limited by the maximum number of MAC-d PDUs that can be included in a single MAC-hs PDU (see 3GPP TS 25.321 [38]).

```

CphyHsSetupParBSCCH = &CphyHsSetupHS_SCCCH;
CphyHsSetupParBSCCH = &CphyHsSetupHS_SCCCH;
CphyHsSetupParBPCCH = &CphyHsSetupHS_BPCCH;
CphyHsSetupParBPCCH = &CphyHsSetupHS_BPCCH;
CmacHsConfigPar = &CmacHsConfigHS_BSCCH;

InterTTI = 1;
MLL = 4800; // 2880 bits/eprocesses
NumOFH_ARQ = 6;
NumOFCH = 5;
ChOfFset = 1;
ModScheme = MOD_QPSK; // Category 12 supports QPSK only.
Atbs = 48; // 12 * (30bits) * 2 (qpsk, 5codes)
NumOFPRFI = 10;
PDUSize = 336;
    
```

UE HS-DSCH Physical Layer category 12:	
HS-PDSCH	Number of processes: <b>6</b> , (alt. 8)
	Process memory size: <b>Split equally between all processes</b>
	Max Data Rate: 1.8 Mbps, (alt. 1.8 Mbps)

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# HSDPA Channels (TS34.108 6.10.2.4.5.2 Interactive or Background/UL: 384 DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

TS25.321 Table 9.2.3.1: Table 0 of values of  $k_{0,i}$  for different numbers of channelization codes and modulation schemes (QPSK and 16QAM)

Combination $i$	Modulation scheme	Number of channelization codes	
0	QPSK	1	1
1		2	40
2		3	63
3		4	79
4		5	92
5		6	102
6		7	111
7		8	118
8		9	125
9		10	131
10		11	136
11		12	141
12		13	145
13		14	150
14		15	153
15	16QAM	1	40
16		2	79
17		3	102
18		4	118
19		5	131
20		6	141
21		7	150
22		8	157
23		9	164
24		10	169
25		11	175
26		12	180
27		13	184
28		14	188
29		15	192

TS25.321 Annex A (normative): HS-DSCH Transport Block Size Table for FDD

Index	TB Size	Index	TB Size	Index	TB Size
1	137	86	1380	171	6324
2	149	87	1405	172	6438
3	161	88	1430	173	6554
4	173	89	1456	174	6673
5	185	90	1483	175	6793
6	197	91	1509	176	6916
7	209	92	1537	177	7041
8	221	93	1564	178	7168
9	233	94	1593	179	7298
10	245	95	1621	180	7430
11	257	96	1651	181	7564
12	269	97	1681	182	7700
13	281	98	1711	183	7840
14	293	99	1742	184	7981
15	305	100	1773	185	8125
16	317	101	1805	186	8272
17	329	102	1838	187	8422
18	341	103	1871	188	8574
19	353	104	1905	189	8729
20	365	105	1939	190	8886
21	377	106	1974	191	9047
22	389	107	2010	192	9210
23	401	108	2046	193	9377
24	413	109	2083	194	9546
25	425	110	2121	195	9719
26	437	111	2159	196	9894
27	449	112	2198	197	10073
28	461	113	2238	198	10255
29	473	114	2279	199	10440
30	485	115	2320	200	10629
31	497	116	2362	201	10821
32	509	117	2404	202	11017
33	521	118	2448	203	11216
34	533	119	2492	204	11418
35	545	120	2537	205	11625
36	557	121	2583	206	11835
37	569	122	2630	207	12048
38	581	123	2677	208	12266
39	593	124	2726	209	12488
40	605	125	2775	210	12713
41	616	126	2825	211	12943
42	627	127	2876	212	13177
43	639	128	2928	213	13415
44	650	129	2981	214	13657
45	662	130	3035	215	13904

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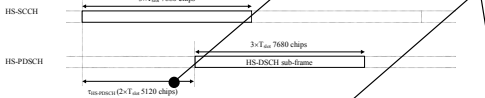


# HSDPA Channels (TS34.108 6.10.2.4.5.2 Interactive or background / UL:384 DL: [max bit rate depending on UE category] / PS RAB + UL:3.4 DL:3.4 kbps SRBs for DCCH)

MD8480C easy\_to\_9.0.pdf A.2.2.7.2 Description of CPHY\_HS\_SETUP\_PAR structure

Member	Description	#1	#2	#3
Offset	Specifies the offset of each channel in [chip]. Specify in multiples of 256.	HS-SCCH offset = P-CPICH offset (=7680)	HS-PDSCH offset = HS-SCCH offset + 5120 (2 slots)	HS-DPCCH offset = HS-SCCH offset + 1280

Figure 35 shows the relative timing between the HS-SCCH and the associated HS-PDSCH for one HS-DSCH sub-frame. The HS-PDSCH starts (HS-PDSCH = 2 Tslot = 5120 chips after the start of the HS-SCCH.



TS25.211 Figure 35: Timing relation between the HS-SCCH and the associated HS-PDSCH.

TS34.108 Table 5.5.1.2.1: HSDPA Downlink Physical Channels Code Allocation for SF=16 Code=0

Code with SF=16	Code with SF=8	Code with SF=4	Note
0	0	0	TS 25.213
1	1	1	TS 25.213
2	2	2	Section 6.1.1b (DSBS)
3	3	3	Section 6.1.1b (DSBS)
4	4	4	Section 6.1.1b (DSBS)
5	5	5	Section 6.1.1b (DSBS)
6	6	6	Section 6.1.1b (DSBS)
7	7	7	Section 6.1.1b (DSBS)
8	8	8	Section 6.1.1b (DSBS)
9	9	9	Section 6.1.1b (DSBS)
10	10	10	Section 6.1.1b (DSBS)
11	11	11	Section 6.1.1b (DSBS)
12	12	12	Section 6.1.1b (DSBS)
13	13	13	Section 6.1.1b (DSBS)
14	14	14	Section 6.1.1b (DSBS)
15	15	15	Section 6.1.1b (DSBS)

The HS-DPCCH shall be spread with code chs as specified in table 1D.

TS25.213 Table 1D: channelisation code of HS-DPCCH

N <sub>max-dpdcch</sub> (as defined in subclause 4.2.1)	Channelisation code C <sub>hs</sub>
0	C <sub>ch,256,33</sub>
1	C <sub>ch,256,64</sub>
2,4,6	C <sub>ch,256,1</sub>
3,5	C <sub>ch,256,32</sub>

```

/*--- HS-SCCH Configuration ---*/
CphyHSSetupParSCCH->Offset = CphyHSSetup_P_CPICH_BTS1.OffSet;
CphyHSSetupParSCCH->TxDiversity = DIVERSITY_OFF;
CphyHSSetupParSCCH->ScrCode = 0x0000009D;

CphyHSSetupParSCCH->NumOfCh = 1;
CphyHSSetupParSCCH->HsCh[0].ChCode = 7;
CphyHSSetupParSCCH->HsCh[1].ChCode = 0;
CphyHSSetupParSCCH->HsCh[2].ChCode = 0;
CphyHSSetupParSCCH->HsCh[3].ChCode = 0;

for(i=0;i<CphyHSSetupParSCCH->NumOfCh;i++){
    CphyHSSetupParSCCH->HsCh[i].DataPower = -183;
    CphyHSSetupParSCCH->HsCh[i].DummyPower = CphyHSSetupParSCCH->HsCh[i].DataPower;
}
CphyHSSetupParSCCH->UEIDMode = UEID_CODE0; // Refer to "Easy to" 5.4 Selection of HS-SCCH
CphyHSSetupParSCCH->HsPowerMode = EACH_MODE;

/*--- HS-PDSCH Configuration ---*/
CphyHSSetupParPDSCH->Offset = CphyHSSetupParSCCH->Offset + 5120;
CphyHSSetupParPDSCH->TxDiversity = DIVERSITY_OFF;
CphyHSSetupParPDSCH->ScrCode = 0x0000009D;

CphyHSSetupParPDSCH->NumOfARQ = NumOfARQ;

for(i=0;i<CphyHSSetupParPDSCH->NumOfARQ;i++){
    CphyHSSetupParPDSCH->ARQInfo[i].IRBQID = 1; // IR-ARQ ID
    CphyHSSetupParPDSCH->ARQInfo[i].IRBufferSize = 8MLs; // IR Buffer Size
}

CphyHSSetupParPDSCH->MinTTI = InterTTI;
CphyHSSetupParPDSCH->HsPowerMode = TOTAL_MODE;

CphyHSSetupParPDSCH->TotalDataPower = -13;
CphyHSSetupParPDSCH->TotalDummyPower = -990;

// Max sending HS-PDSCH with no data
CphyHSSetupParPDSCH->ModScheme = MOD_16QAM;
CphyHSSetupParPDSCH->HsPowerMode = CHOFFSET;
CphyHSSetupParPDSCH->ChOffset = CHOFFSET;
for(i=0;i<CphyHSSetupParPDSCH->NumOfCh;i++){
    CphyHSSetupParPDSCH->HsCh[i].ChCode = 1 + i;
    CphyHSSetupParPDSCH->HsCh[i].Initial_PN15 = 1 + i;
}

CphyHSSetupParPDSCH->MaxPower = 0;
CphyHSSetupParPDSCH->MinPower = 999;
CphyHSSetupParPDSCH->TxDiversity = DIVERSITY_OFF;

/*--- HS-DPCCH Configuration ---*/
CphyHSSetupParDPCCH->Offset = CphyHSSetupParSCCH->Offset + 1280;
CphyHSSetupParDPCCH->ScrCode = 0x01000000;
CphyHSSetupParDPCCH->HsPowerMode = 64;
CphyHSSetupParDPCCH->HsPowerThreshold = -20;
CphyHSSetupParDPCCH->HsPowerThreshold > HS_DPCCH_Power : HsPowerThreshold > HS_DPCCH_Power : DTX else :ACK/NACK */
CphyHSSetupParDPCCH->AckNackRepfactor = 1;
    
```

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# HSDPA Channels (TS34.108 6.10.2.4.5.2 Interactive or Background/UL: 384 DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps SRBs for DCCH)

TS34.121 Table 9.2.4: Node-B Emulator Behavior in response to ACK/NACK/DTX

HS-DPCCH ACK/NACK Field State	Node-B Emulator Behavior
ACK	ACK: new transmission using 1 <sup>st</sup> redundancy and constellation version (RV)
NACK	NACK: retransmission using the next RV (up to the maximum permitted number of RVs)
DTX	DTX: retransmission using the RV previously transmitted to the same H-ARQ process

```

/*--- MAC-hs ---*/
CmacHSConfigPar->NumOfARQ = NumOfARQ;
CmacHSConfigPar->NumOfRetransmission = 3; // Maximum Retransmission */

/* Retransmission parameter for NACK */
CmacHSConfigPar->Retrans_QPSK[0].Nack_Xrv = 0; // Xrv for new Transmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[1].Nack_Xrv = 1; // Xrv for 1st Retransmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[2].Nack_Xrv = 2; // Xrv for 2nd Retransmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[3].Nack_Xrv = 3; // Xrv for 3rd Retransmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[0].NackDeltaPower = 0; // Delta Power for new Transmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[1].NackDeltaPower = 0; // Delta Power for 1st Retransmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[2].NackDeltaPower = 0; // Delta Power for 2nd Retransmission by NACK received */
CmacHSConfigPar->Retrans_QPSK[3].NackDeltaPower = 0; // Delta Power for 3rd Retransmission by NACK received */

/* Retransmission parameter for DTX */
CmacHSConfigPar->Retrans_QPSK[0].Dtx_Xrv = 0; // not use */
CmacHSConfigPar->Retrans_QPSK[1].Dtx_Xrv = -1; // Xrv for 1st Retransmission by DTX received, -1 means previous Xrv */
CmacHSConfigPar->Retrans_QPSK[2].Dtx_Xrv = -2; // Xrv for 2nd Retransmission by DTX received, -1 means previous Xrv */
CmacHSConfigPar->Retrans_QPSK[3].Dtx_Xrv = -3; // Xrv for 3rd Retransmission by DTX received, -1 means previous Xrv */
CmacHSConfigPar->Retrans_QPSK[0].DtxDeltaPower = 0; // not use */
CmacHSConfigPar->Retrans_QPSK[1].DtxDeltaPower = 0; // Delta Power for 1st Retransmission by DTX received */
CmacHSConfigPar->Retrans_QPSK[2].DtxDeltaPower = 0; // Delta Power for 2nd Retransmission by DTX received */
CmacHSConfigPar->Retrans_QPSK[3].DtxDeltaPower = 0; // Delta Power for 3rd Retransmission by DTX received */

/* Retransmission parameter for ACK */
CmacHSConfigPar->Retrans_16QAM[0].Ack_Xrv = 0; // Xrv for new Transmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[1].Ack_Xrv = 1; // Xrv for 1st Retransmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[2].Ack_Xrv = 2; // Xrv for 2nd Retransmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[3].Ack_Xrv = 3; // Xrv for 3rd Retransmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[0].AckDeltaPower = 0; // Delta Power for new Transmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[1].AckDeltaPower = 0; // Delta Power for 1st Retransmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[2].AckDeltaPower = 0; // Delta Power for 2nd Retransmission by NACK received */
CmacHSConfigPar->Retrans_16QAM[3].AckDeltaPower = 0; // Delta Power for 3rd Retransmission by NACK received */

/* Retransmission parameter for DTX */
CmacHSConfigPar->Retrans_16QAM[0].Dtx_Xrv = 0; // not use */
CmacHSConfigPar->Retrans_16QAM[1].Dtx_Xrv = -1; // Xrv for 1st Retransmission by DTX received, -1 means previous Xrv */
CmacHSConfigPar->Retrans_16QAM[2].Dtx_Xrv = -2; // Xrv for 2nd Retransmission by DTX received, -1 means previous Xrv */
CmacHSConfigPar->Retrans_16QAM[3].Dtx_Xrv = -3; // Xrv for 3rd Retransmission by DTX received, -1 means previous Xrv */
CmacHSConfigPar->Retrans_16QAM[0].DtxDeltaPower = 0; // not use */
CmacHSConfigPar->Retrans_16QAM[1].DtxDeltaPower = 0; // Delta Power for 1st Retransmission by DTX received */
CmacHSConfigPar->Retrans_16QAM[2].DtxDeltaPower = 0; // Delta Power for 2nd Retransmission by DTX received */
CmacHSConfigPar->Retrans_16QAM[3].DtxDeltaPower = 0; // Delta Power for 3rd Retransmission by DTX received */

// Refer to "Easy to" 5.2.5 Settings for retransmission
    
```

TS34.121 Table 9.2.1A.1: Test Parameters for Testing QPSK FRCs H-Set 1/H-Set 2/H-Set 3

Parameter	Unit	Test 1	Test 2	Test 3	Test 4
Phase reference	dBm/3.84 MHz		P-CPICH		
			-60		
Redundancy and constellation version coding sequence			{0,2,5,6}		
Maximum number of HARQ transmission			4		

Note: The HS-SCCH-1 and HS-PDSCH shall be transmitted continuously with constant power. HS-SCCH-1 shall only use the identity of the UE under test for those TTI intended for the UE.

TS34.121 Table 9.2.1A.3: Test Parameters for Testing 16QAM FRCs H-Set 1/H-Set 2/H-Set 3

Parameter	Unit	Test 1	Test 2	Test 3	Test 4
Phase reference	dBm/3.84 MHz		P-CPICH		
			-60		
Redundancy and constellation version coding sequence			{6,2,1,5}		
Maximum number of HARQ transmission			4		

Note: The HS-SCCH-1 and HS-PDSCH shall be transmitted continuously with constant power. HS-SCCH-1 shall only use the identity of the UE under test for those TTI intended for the UE.

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# HSDPA Channels (TS34.108 6.10.2.4.5.2 Interactive or Background/UL: 384 DL: [max bit rate depending on UE category]/PS RAB + UL: 3.4 DL: 3.4 kbps Serbs for DCCH)

Higher layer	RAB/Signalling RB	RAB
RLC	Logical channel type	DTCH
	RLC mode	AM
	Payload sizes, bit	320 (alt. 640)
	Max data rate, bps	depends on UE category
	AMD PDU header, bit	NOTE1 16
MAC	MAC-d header, bit	0
	MAC multiplexing	N/A
	MAC-d PDU size, bit	336 (alt. 656)
	MAC-hs header fixed part, bit	21
Layer 1	TrCH type	HS-DSCH
	TTI	2 ms
	Coding type	TC
	CRC, bit	24

NOTE: The peak throughput may be limited by the maximum number of MAC-d PDUs that can be included in a single MAC-hs PDU (see 3GPP TS 25.321 [38]).

```

CrhcConfigPar = #Packet_CrhcConfig_DCCH;
memset( CrhcConfigPar, 0, sizeof(CRHC_CONFIG_PAR) );
CrhcConfigPar->NumOfEPUs = 1;
CrhcConfigPar->PU_LengthTM = 244;
CrhcConfigPar->PU_LengthUM = 328;
CrhcConfigPar->PU_LengthAM = 320;
    
```

```

CmacHsConfigPar->NumOfPriorityQueue = 1;
CmacHsConfigPar->NumOfLoch[0] = 1;

/* Loch Info */
CmacHsConfigPar->LochHsInfo[0][0].Loch = 0;
CmacHsConfigPar->LochHsInfo[0][0].LochNo = 0;
CmacHsConfigPar->LochHsInfo[0][0].CTLength = 0;
CmacHsConfigPar->LochHsInfo[0][0].CTValue = 0;
CmacHsConfigPar->LochHsInfo[0][0].UEIDIndex = 0;
CmacHsConfigPar->LochHsInfo[0][0].UEID = 0x1234; /* UE ID // Match to L3 Message */
CmacHsConfigPar->LochHsInfo[0][0].UEIDType = UEID_H_RNTI;
    
```

MD8480C easy\_to\_9.0.pdf A.2.2.3.2 Description of CMAC\_HS\_CONFIG\_PAR structure

Field	Description
Loch	Specifies the type of Logical Channel. Details of each parameter are described below.
LochNo	Specifies the channel number of Logical Channel.
Priority	Specifies the priority of Logical Channel. Currently disabled.
CTLength	Specifies the length of CT field in MAC Header. Specify 0 or 4. (Set to 0 when not using CT field.)
CTValue	Specifies the value of CT field in MAC Header. Can be set to 0-15.
UEIDIndex	Specifies 0-7.
UEIDType	Specifies the value of UEID Type field.
UEID	Specifies the value of UEID Field.

```

/* Queue Info */
// Refer to "Easy to..." 5.2.5.2 MAC-hs Tx Window Size
CmacHsConfigPar->QueueInfo[0].MACWindowSizeMode = 16;
CmacHsConfigPar->QueueInfo[0].QueueID = 0;
CmacHsConfigPar->QueueInfo[0].NumOfPFI = NumOfPFI;
for (i=0; i<CmacHsConfigPar->QueueInfo[0].NumOfPFI; i++)
{
    CmacHsConfigPar->QueueInfo[0].TFRI[i].NumOfPDU = 1 + i;
    CmacHsConfigPar->QueueInfo[0].TFRI[i].NumOfCh = NumOfCh;
    CmacHsConfigPar->QueueInfo[0].TFRI[i].Xms = ModScheme;
    CmacHsConfigPar->QueueInfo[0].TFRI[i].Xkbs = Xkbs;
    CmacHsConfigPar->QueueInfo[0].TFRI[i].CodeOffset = CodeOffset;
}
CmacHsConfigPar->QueueInfo[0].PDUSize[0] = PDUSize;
    
```

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