

Understanding Jitter in Transport Networks

CMA5000

XTA module (eXtended Transport Analysis)

Introduction

Modern Telecommunication networks will still be running in the years ahead with the classical machinery of the synchronous SONET/SDH infrastructure throughout the world. While great care is devoted to warrant a very high quality of transport (at the physical level), in the real world of day-to-day installation, commissioning and maintenance activities things are not necessarily running smooth. Network clock synchronization, wander and timing instabilities are only a few examples of recurrent phenomena likely to pester network engineers in charge of these broadband networks. Fast timing instabilities in the clocks and data lines are commonly designated by the term Jitter, while the term Wander addresses the slower fluctuations affecting these elements.

The object of this technical note is to explain jitter phenomenon and present the common techniques used to qualify and control it. Another technical note elaborates in more details on wander problematic.

What is jitter, what are its causes and its consequences

Jitter: what is it?

Jitter represents the time fluctuations in the rising and falling edges of digital pulses. While we generally mentally assume that, say, the rising edges in a 2,5G clock occur exactly every 400 ps, various phenomena blur this ideal picture and fluctuations (phase variations) of several ps around the “official” rising times happen. The question then is to constrain these timing imperfections within specific limits in order to avoid trouble.

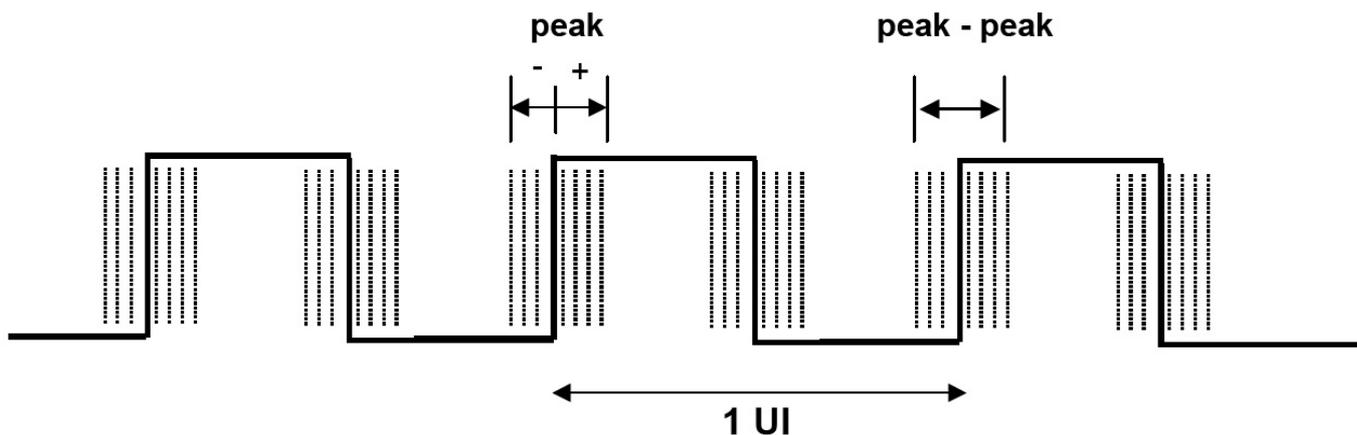


Figure 1. Jittered clock signal

What are the causes of jitter?

Impulsive noise or cross talk on transmitted signals usually causes high frequency jitter. The same applies for thermal noise in a clock circuitry. The regular repetition of digital patterns causes what is called pattern-dependent systematic jitter. A good example of that are the A1/A2 framing bytes in SONET/SDH streams: these bytes are not scrambled and the same pattern therefore occurs at 8kHz frequency thereby creating some form of jitter.

There are other causes in SONET/SDH networks, like mapping-demapping jitter and pointer induced jitter. When we insert for instance into a VC12 an E1 signal that runs 10 ppm faster than the SDH node, E1 chunks are encapsulated into VC12 multi-frames in a way to cope with the rate difference between the tributary and the network. Most chunks will be 1024 bit long but one out of 100 will have 1025 bits. In another words the information stream is not constant. Upon retrieving this E1 these time discontinuities in the E1 info will inevitably generate jitter on the extracted E1: this is called mapping-demapping jitter.

Pointer-induced jitter is more serious. SONET/SDH networks with bad network synchronization must proceed to what is called pointer adjustments. These pointer movements generate gaps in the information flow and when tributaries are extracted from the synchronous network they again inevitably pick up some jitter fluctuations.

What are the consequences of jitter?

Maybe the easiest way to understand why jitter is dangerous is to imagine that these time fluctuations occur randomly and change very quickly in time. The digital detection process on such an input port will use a sampling clock that will look very much like the dark regular line on Figure 1. This is so because the internal clock circuitry will filter out these high frequency fluctuations. So the sampling instants (for the detection) will fall very regularly but they won't fall right in the middle of the data (jittered) pulses. If their jitter is too high this situation will likely cause bit errors.

Another way to look at it is to imagine how this high frequency jitter will affect the eye diagram of reception process. It will look as shown on the Figure 2, with a narrowed eye opening, something likely to create errors.

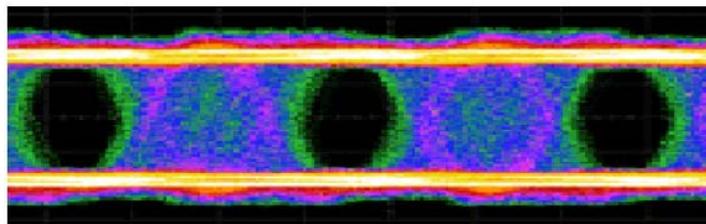


Figure 2. Jittered eye diagram

This example was focused on a high frequency case but a large low frequency jitter is just as dangerous as it may destabilize the reception circuitry. Furthermore, large jitter bursts on tributaries are liable to cause a loss of framing (for example on a DS1 signal), thereby triggering a loss of information and impacting the quality of service. Examples of services that typically suffer from severe jitter are: encrypted text, Facsimile, Video, voice band data, compressed Audio and cellular trunk lines.

Jitter terminology

Timing fluctuations are analysed with a jitter detector, whose circuitry continually yields the evolution of the phenomenon.

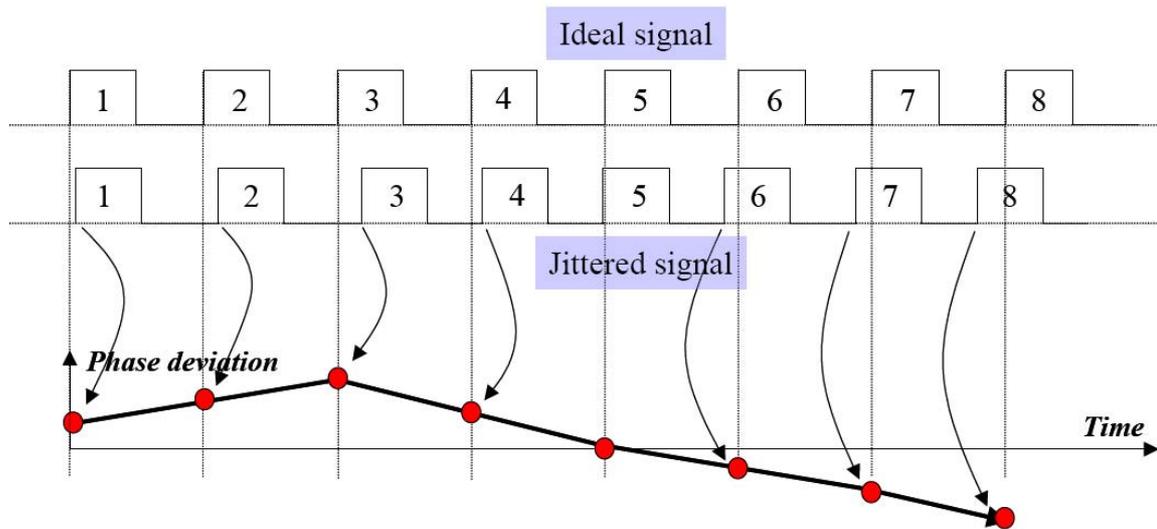


Figure 3. Output of jitter detector circuit

In order to characterize jitter the detector output is pass-band filtered and a peak-to-peak or rms measurement is carried out on the resulting output. The jitter unit is called Unit Interval (UI). A UI is simply a bit period for the considered rate.

Peak-to-peak jitter is written UI pp and root mean square jitter UI rms. Both quantities are used in jitter tests. UI pp gives a measure of worst case jitter while UI rms is helpful when one wants to cumulate jitter in a chain of network elements.

Network interface	Bit Rate	UI (Unit Interval)	Network Interface	Bit Rate	UI (Unit Interval)
PDH / T-Carrier	1.5 M (DS1)	0.65 μ s	SDH / SONET	STS-1	19.29 ns
	2 M (E1)	0.49 μ s		STM-1/OC-3	6.43 ns
	34 M (E3)	29.10 ns		STM-4/OC-12	1.61 ns
	45 (DS3)	22.35 ns		STM16/OC-48	401.9 ps
	140 (E4)	7.18 ns		STM-64/OC-192	100.5 ps

Figure 4. Unit Interval (UI) values per bit rate

The reason why each jitter measurement is associated to a filter is that jitter's spectrum is quite broad and not at all confined to a small frequency band, as reminded in figure 5. Figure 6 shows the 2 filters used for UIpp characterization.

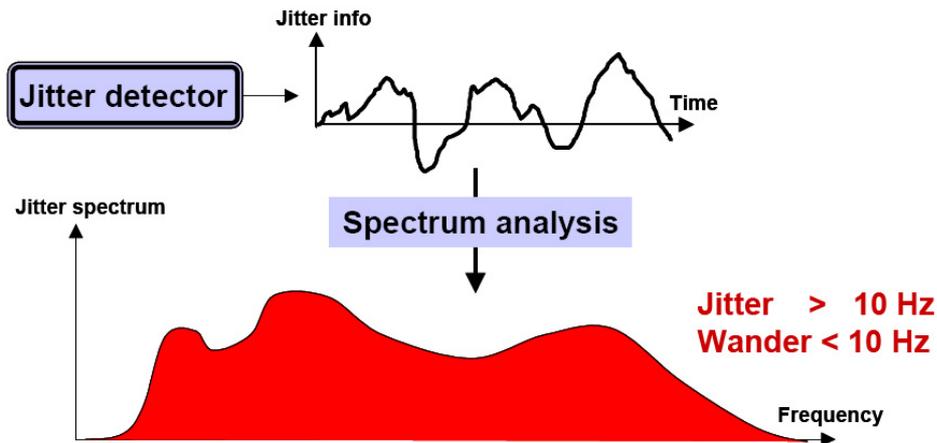


Figure 5. Phase deviation amplitude spectrum

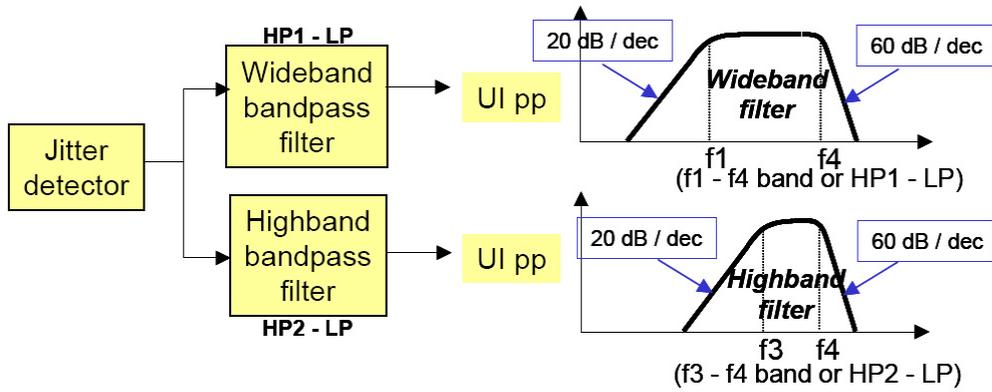


Figure 6. Wide band and High band pass filters used for measuring jitter

Each interface rate has normalized HP1-LP & HP2-LP filters. Here HP stands for high pass and LP for low pass. The standard procedure to characterize peak-to-peak jitter is to record the two UIpp values after 60 seconds. For UI rms measurements another pass band filter is applied with 12 kHz high pass and the same LP low pass filter.

For example, at STM16 – OC-48 level, UI pp is gauged in the bands [5 kHz, 20 MHz] and [1MHz , 20 MHz] and UI rms in the band [12 kHz , 20 MHz]. These values appear in the CMA5000 XTA GUI jitter analysis screen as shown on figure 7.

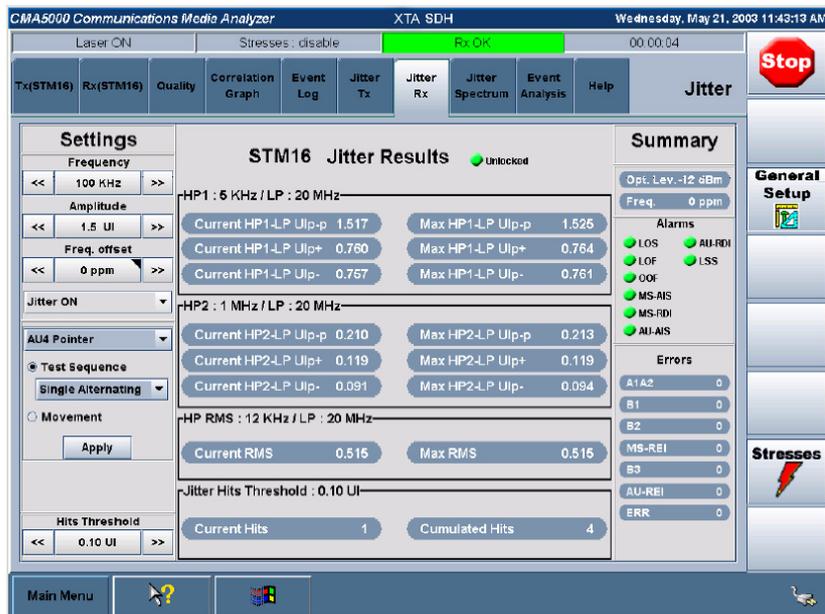


Figure 7. Simultaneous jitter results through HP1 and HP2 filters with CMA5000-XTA

Standard jitter measurements and associated limits / templates

There are a few basic tests that need to be carried out if one wants to warrant full compliance of interfaces and networks as far as jitter is concerned. These are presented below:

Intrinsic jitter

Nothing being perfect, any output interface is jittery. At the output of a circuit pack we must make a distinction between two different cases: either this unit is running with a very stable clock or this clock is itself likely to be jittery. Obviously the first case represents the jitter floor level and this is called “intrinsic jitter”.

When units are validated, their “intrinsic jitter” is measured and compared to the standard limits. As outlined above, this means running them in free mode or slaved by any very stable independent clock and registering the UI pp data after one minute. The standard limits as per ITU-T are as displayed in Table 1. For instance at STM16 level limits are 500 mUI pp in the [5 kHz, 20 MHz] wideband and 100 mUI pp in the [1 MHz, 20 MHz] high band. Any interface with results above these figures would not be compliant.

Bit Rate	Wideband UI pp	Wideband limit	High band UI pp	High band limit
2M	0.05	20 Hz - 100 KHz	x	18 KHz - 100 KHz
34M	0.05	100 Hz - 800 KHz	x	10 KHz - 800 KHz
140M	0.05	200 Hz - 3,5 MHz	x	10 KHz - 3,5 MHz
STM-1 (opt)	0.5	500 Hz - 1,3 MHz	0.1	65 KHz - 1,3 MHz
STM-4	0.5	1 KHz - 5 MHz	0.1	250 KHz - 5 MHz
STM-16	0.5	5 KHz - 20 MHz	0.1	1 MHz - 20 MHz
STM-64	0.5	20 KHz - 80 MHz	0.1	4 MHz - 80 MHz

Table 1. Standard intrinsic jitter limits as per ITU-T

Maximum permissible output jitter

In real world network interfaces are not necessarily run with a jitter less clock. As a matter of fact many telecom facilities usually derive their clocking from one incoming high speed line and therefore pick up jitter in the process. The ITU-T has defined upper limits for jitter, ones that must never be exceeded whatever the network details. These are shown in the Table 2.

Network Interface	Standard	Bit rate	Wideband UI pp	Wideband limit	High band UI pp	High band limit
PDH	ITU-T G.823	2M (E1)	1.5	20 Hz - 100 KHz	0.2	18 KHz - 100 KHz
		8M	1.5	20 Hz - 400 KHz	0.2	3 KHz - 400 KHz
		34M (E3)	1.5	100 Hz - 800 KHz	0.15	10 KHz - 800 KHz
		140 (E4)	1.5	200 Hz - 3,5 MHz	0.075	10 KHz - 3,5 MHz
SDH	ITU-T G.825	STM-1 (opt)	1.5	500 Hz - 1,3 MHz	0.15	65 KHz - 1,3 MHz
		STM-4	1.5	1 KHz - 5 MHz	0.15	250 KHz - 5 MHz
		STM-16	1.5	5 KHz - 20 MHz	0.15	1 MHz - 20 MHz
		STM-64	1.5	20 KHz - 80 MHz	0.15	4 MHz - 80 MHz

Table 2. Maximum permissible output jitter

For instance at STM16 level these network limits are 1500 mUI pp in the [5 kHz, 20 MHz] and 150 mUI pp in [1 MHz , 20 MHz]. As usual, these measurements are carried out in one minute. Any situation violating these limits would be cause for concern and would require searching the cause of the problem (circuit pack, local clock unit, clock distribution, etc...).

Jitter tolerance

All input port circuitries must be able to function in the presence of jitter on the received signals. One says that they must tolerate jitter (up to a certain point). This minimum tolerance has been standardized. Unfortunately ITU and North America specifications are different on this and other issues. We show here (figure 8) a 2.5 G level tolerance measurement and the associated Bellcore standard (in red).

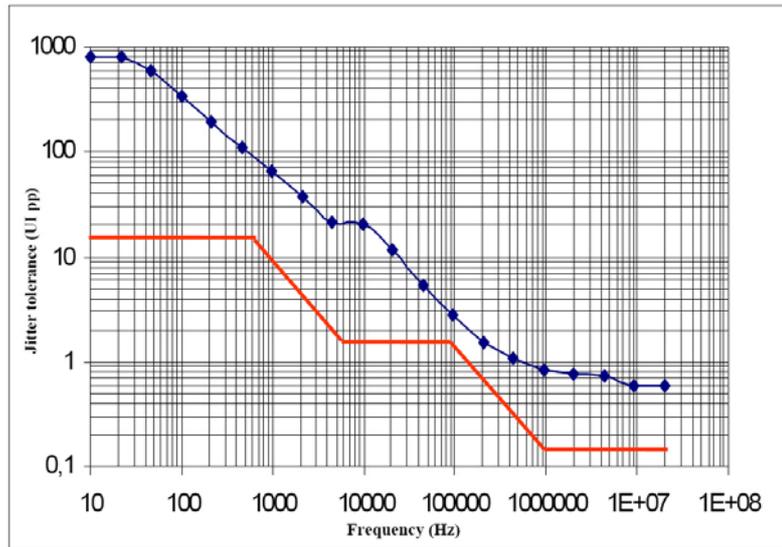


Figure 8. Example of 2.5G jitter tolerance measurement compare to Bellcore mask (in red)

Its meaning is quite straightforward:

The port accepts up to 60 UI pp jitter with 1000 Hz frequency, 20 UI pp at 10 kHz, 2.5 UI pp at 100 kHz, 0.9 UI pp at 1 MHz and 0.6 UI pp at 20 MHz, for instance. In all cases this is better than the template data and therefore the corresponding ports are compliant. That sort of jitter tolerance checking must be done at least during manufacturing.

The tolerance measurement is best carried out automatically. The tester generates jitter frequency stresses (applied to the DUT device under test) and searches the amplitude limit beyond which the DUT input port starts experiencing errors. For instance in the example above, when the tester reaches 0.6 UI pp at 20 MHz the OC-48 receiver identifies B2 errors, which are signalled in the outgoing OC-48 line with the REI-L counter SONET scheme. The tester only needs to analyse this return line to know the jitter limit has been reached. It then proceeds to stress the DUT at another frequency (see figure 9).

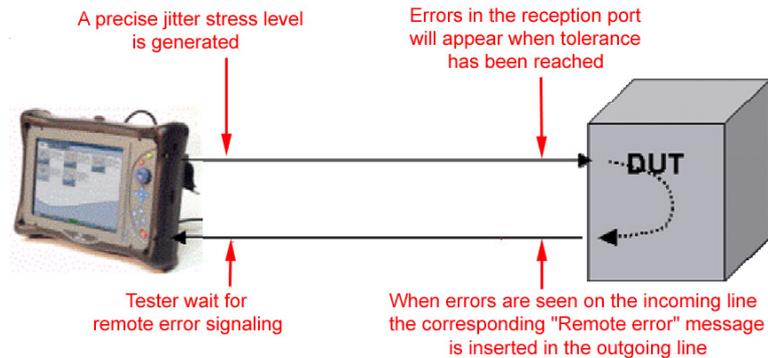


Figure 9. Automatic jitter tolerance measurement

Jitter transfer

Jitter transfer basically concerns regenerators. These equipments lock themselves onto the incoming signal but their PLL circuitry does not phase out jitter altogether. Its internal filter effectively attenuates only the high frequency content. On the other hand, low frequency jitter may be slightly amplified, which will show in the outgoing line. This “jitter transfer” (from incoming to outgoing line) must be limited because a chain of regenerators could otherwise amplify jitter in an uncontrollable way.

Figure 10 shows a jitter transfer measurement done at OC-48 level along with the Telcordia template for regenerators (in red). We see that above 2 MHz the template has a 20 dB per decade slope while low frequencies template is flat (at 0.1 dB). This measurement is a good example of a typical good jitter transfer case. In all cases the transfer curve must be below the template. This measurement is always carried out automatically but requires a pre calibration to guarantee accurate results.

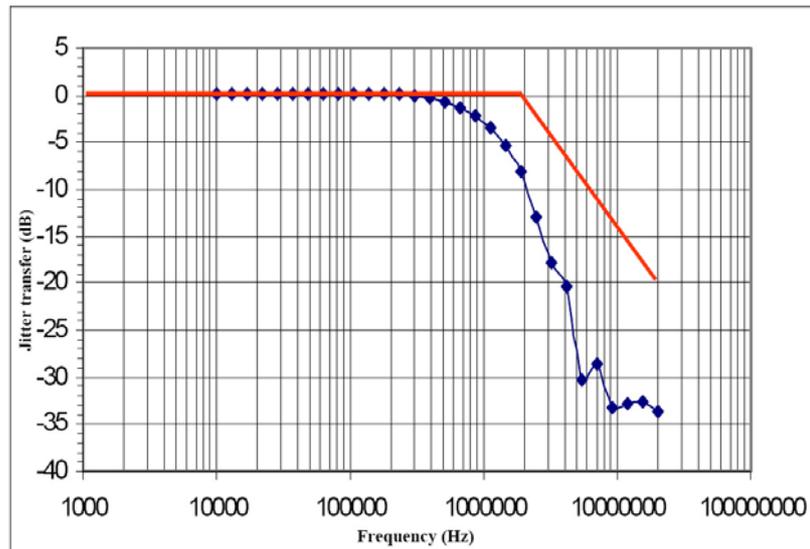


Figure 10. OC-48 jitter transfer measurement.

Jitter on tributaries travelling on SDH/SONET networks

SDH & SONET technology is great but it actually does not always treat its payload fairly! Even with a jitterless synchronous line you may end up extracting, say, a 2M tributary trunk line with jitter. Why? Because of pointer activity within the SDH/SONET network. Extracting (dropping) a 2M from a VC12 with pointer movements will inevitably render this 2M jittery. This is called pointer-induced jitter. Note that there is also another jitter type called mapping-demapping jitter but it is usually less severe. Pointer-induced jitter is attenuated as much as possible by a circuit called “desynchroniser” in the extracting unit. In order to make sure that this phenomenon is acceptable, it is best to try it, if at all possible. This is always done generating pointer activity with a few normalized pointer sequences. These create a stress on the tributary extraction process and the corresponding tributary jitter is analysed and compared to standard limits (as defined in G.783 in the SDH case).

CMA5000 XTA jitter screens

The CMA5000 XTA graphical user interface is particularly handy to carry out the jitter measurements. This section outlines its features.

Manual Tx/Rx jitter window

The jitter generation (Tx) and jitter analysis (Rx) windows are respectively shown in Fig. 11 and 7. The left column (present in Tx and Rx) shows the jitter stress generation parameters (frequency, amplitude UI pp) as well as the rate offset in ppm. The lower part is used for pointer sequence activity in the SDH/SONET cases, something important when testing the pointer-induced jitter on the embedded tributaries. The hit threshold is used mainly to monitor high UI pp jitter occurrence.

The central part of Tx window displays the applied jitter stress. It appears clearly on the frequency / amplitude graph superimposed with the relevant tolerance template for the interface under test. This is a useful guideline since applying a jitter stress only makes sense if one knows what minimum stress the DUT is supposed to handle. Here it shows as a blue line and the current stress corresponds to the green dot (100 kHz @ 1.5 UI pp on Figure 11). Another information, the maximum stress capability of the tester, is also displayed: this is the upper curve in the Tx window.



Figure 11. Jitter generation configuration with CMA5000 XTA

The central part of the analysis (Rx) window (refer to Fig.7) displays all the important information at the same time, which spares the trouble of having to change windows and menus in order to understand what's going on or capture the analysis again after changing the analysis filter. Here all is available at a single glance.

The analysis in all three bands (HP1-LP, HP2-LP and 12kHz-LP) yields the UI pp and UI rms info in the current second and the maximum data recorded since starting the measurement.

The right column is also common to Tx and Rx windows. It displays the situation at the interface alarm and error levels in order to render the appraisal of the situation easier for the operator.

Jitter tolerance windows

Figures 12 and 13 respectively show the full and fast tolerance windows. Both have a common left column displaying the relevant jitter tolerance settings.

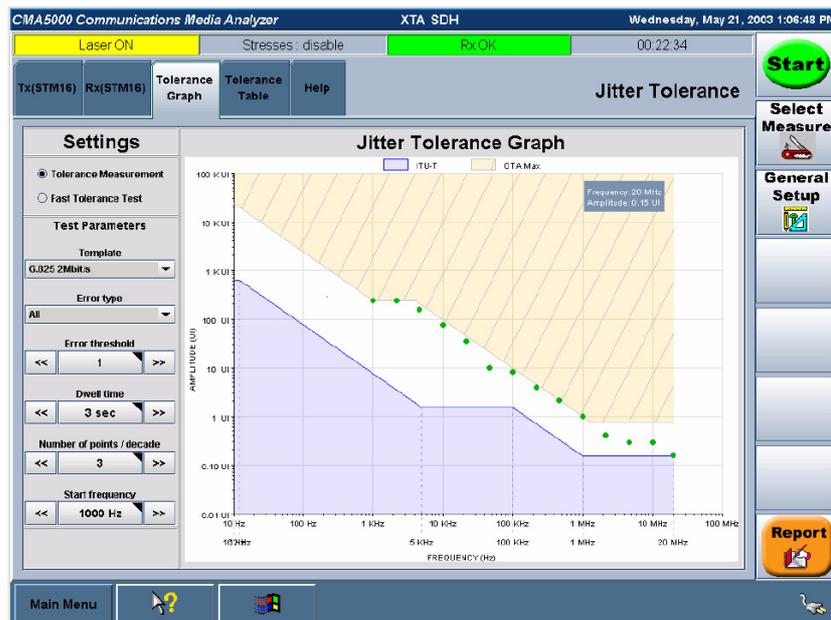


Figure 12. Full jitter tolerance measurement with CMA5000 XTA.

The error type indicates the signalling used to track the onset of errors during the tolerance measurement. In most cases the error type would be typically a remote signalling like MSREI.

In each stress trial the equipment waits a certain time (commonly called gate time or dwell time). If during this interval no error was signalled at the DUT input, the applied stress is deemed below the tolerance. The same applies too as long as the number of errors is below the parameter “error threshold” within this dwell time.

In the full tolerance search, the software must then go on probing the DUT with a higher stress in order to find out the onset of errors. This is done at different frequencies. In Fig. 12 just 3 jitter points were scanned in each decade. The green dots show the maximum jitter stimuli that the DUT accepted in this instance.

The only problem with full tolerance is that it takes time : if you scan 3 decades with 3 points per decade, with an average of 5 iterations on each frequency and 5 seconds waiting at each trial (dwell time) you need almost 6 minutes altogether.

A more pragmatic approach consists in doing a fast tolerance (as per Fig. 13). The software will not try and find the real jitter limit but will only do one trial per frequency: with a fast tolerance parameter set to 0% , it will actually follow the selected template and try it on the DUT. The idea here is just checking that the DUT passes the test. It is also good practice to introduce a margin here, say 50 % above the template. The stresses will be 50 % higher (compared to the 0 % case) and if the DUT passes the test, so much the better.

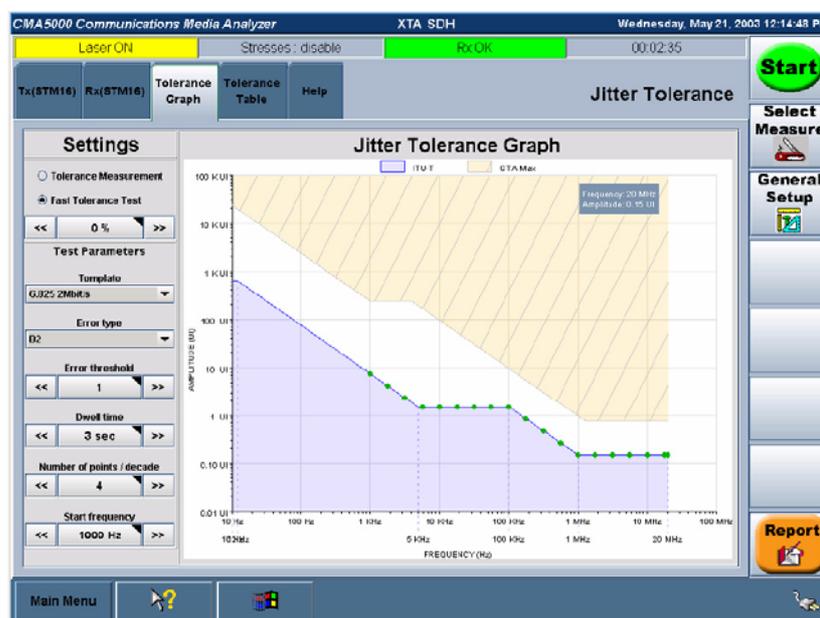


Figure 13. Save time with the fast tolerance test of the CMA5000 XTA

Jitter transfer windows

The Figures 14 and 15 show the user interface on jitter transfer. The calibration phase (Fig. 14) means we first perform jitter measurements looping the tester on itself. This will allow accurate jitter transfer after inserting the DUT in-between. Here the “dwell time” parameter is the time dedicated to each jitter measurement. Its setting is a matter of trade-off: a large interval will give very accurate transfer data but after a long time.

After running the measurements the transfer data (in dB) are displayed with the relevant background template. The green dots on the left in Figure 15 correspond to data close to 0 dB and below the 0.1 dB template limit in the flat band area.

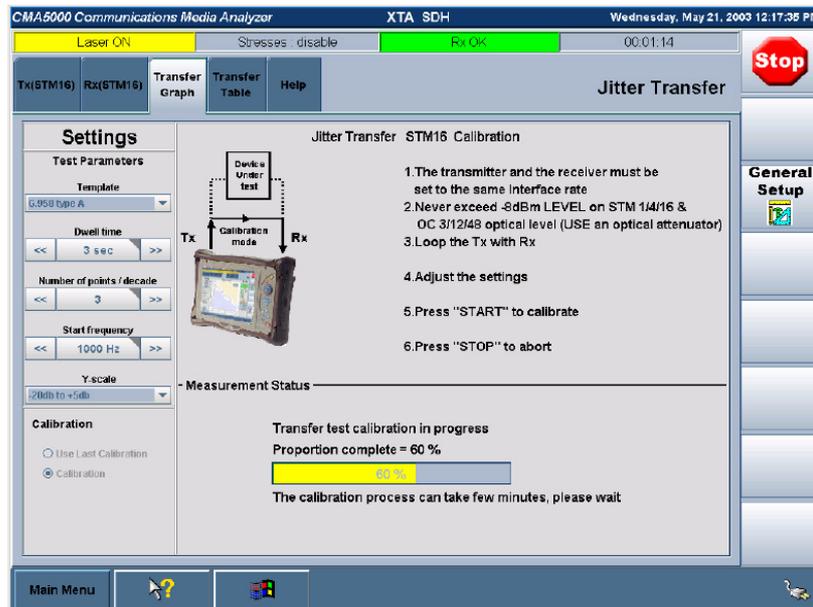


Figure 14. Calibration phase before measuring jitter transfer



Figure 15. Jitter transfer graph on CMA5000 XTA

Conclusion

This note presented the main features of Anritsu XTA jitter generation and analysis option. It first gave a background on the problematic of jitter and then illustrated them with the application's GUI windows. Jitter measurements are usually considered quite tedious but with this new solution many potential users should and certainly will change their mind on that issue.



Specifications are subject to change without notice.

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