Millimeter-wave Power Control for Network Analysis

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[Summary] Millimeter network analysis and related measurements are increasingly needed to support 6G and other applications. An important part of these measurements may include accurate, leveled power control for stability, to keep a device under test in its linear range of operation, or to allow for accurate quasi-linear and nonlinear measurements. Achieving this control over wide ranges at mm-wave frequencies is challenging for reasons of detection noise and linearity, modulation stability and complex leveling loop dynamics. Some power leveling architectures will be explored including methods to obtain >50 dB of control range to over 200 GHz with stability better than 0.5 dB under a variety of conditions.

1 Introduction

Millimeter-wave applications continue to be important including those in the areas of imaging, point-to-point communications, and communications in the form 6G and similar efforts[e.g.,1)-5)]. In most of these applications, vector network analysis (VNA) is an important development and production measurement and one aspect of interest is power control.

For device level test[e.g.,6)] at mm-wave frequencies, the required incident power levels to avoid compression may be very low (for example, < −30 dBm for some W-band-capable transistors) so accurate power control may be required even for small signal analysis. As higher frequency power amplifier development proliferates[e.g.,3), 7)], power control is even more critical for quasi-linear and nonlinear quantities such as compression (including AM/AM and AM/PM), intermodulation distortion, and even error vector magnitude (when studied in a modulated VNA context). Of course, many of these control/leveling concerns also apply to any mm-wave signal generation platform as well.

At microwave frequencies, achieving such control has been less of a concern since a relatively high-performing power leveling system at those frequencies can often be relatively straightforward to implement. A classical structure is shown in Figure 1 where a broadband detector samples the output power, the output of which is fed to a difference node where the value is compared against some target (represented by the digital-to-analog converter (DAC)). The resulting difference is applied to an integrator or similar structure and the final signal applied to a voltage-variable attenuator or amplifier ('modulator' will be the general term used in this paper).

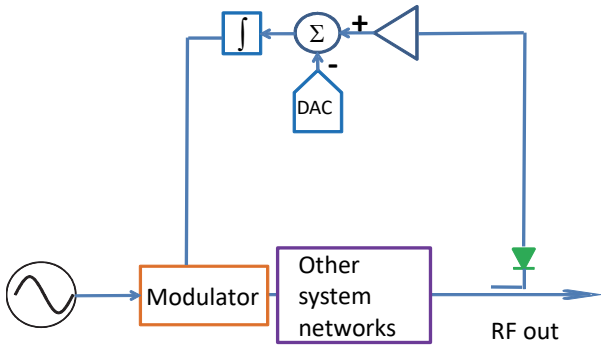

Figure 1 A heavily simplified block diagram of a classical microwave power leveling loop is shown here.

In mm-wave systems, a number of aspects of this structure need to be revisited as performance changes. Overall insertion loss is more of a concern as power is more expensive to obtain, RF bandwidths are much larger so the noise energy incident on the detectors increases, a given detector or modulator technology may no longer be appropriate for the given frequency range, and the nature of the interior loop elements may no longer be appropriate. In this paper, some of the architectural and structural choices in a mm-wave power control loop will be studied with the objective of obtaining wide power control ranges, adequate power accuracy and stability and minimal unintended state changes of the (potentially nonlinear) DUT.

2 Architectural options

There are many possible general structures available including the choice of whether the control loop is fully analog,

mostly in digital hardware or mostly in software. For the (usually) required analog portions, there are some choices to be made:

Where is detection happening? After all multiplication stages or before one or more of the final stages?

How is detection being done? One or more broadband detectors (log or otherwise), heterodyne detection, direct digitization….?

Where is modulation (or power control) being done? After the last multiplication stage or earlier?

At microwave frequencies, the classical approach of detection and modulation at the latest stage possible (to minimize errors and maximize stability) is often done and broadband diode detectors or direct digitization may be employed. At mm-wave frequencies, these choices run into complications as was alluded to in the introduction.

Broadband detection at the final frequency implies a wide noise bandwidth which will reduce the effective detectable power range. Multiple detection stages can be used as in some power sensors[e.g.,8] but even this has its limits without compromising stability and accuracy. Detector linearity at these frequencies can also be a challenge although corrections are possible[e.g.,9]. Direct digitization may not be currently practical at 100+ GHz with presently available technologies. Broadband or direct detection prior to the final multiplication stage is a possibility as that may reduce the design to a microwave problem. This approach does, however, leave the conversion characteristics of the final multiplier outside the loop so drift may increase and there may be heightened sensitivity of the output power if the P_{out}-P_{in} slope of the multiplier is steep (see Figure 2).

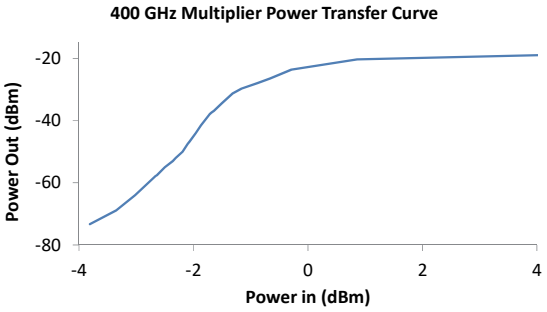

Figure 2 The P_{out}-P_{in} slope of mm-wave multipliers can vary widely and may become very steep when backed-off (note the different x and y scales).

Heterodyne detection is an interesting possibility since this permits detection at the highest frequencies but without the noise bandwidth or technological complications of other approaches. In this approach (see Figure 3), a coupled portion of the output drive is downconverted and filtered to MHz or lower GHz frequencies before being directly detected (possibly with a log detector)[e.g.,10]. The loss budget of the coupler + downconverter does need to be carefully considered but the losses are often outweighed by the 20-50 dB increase in detection range available at the filtered and lower output frequencies.

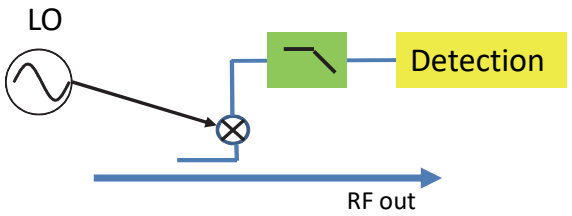

Figure 3 A heterodyne method of level detection can sometimes improve mm-wave power leveling. The downconverter and LO may be part of the measurement receiver proper or may be separate.

Final stage modulation can be a challenge because of high minimum insertion losses at mm-wave frequencies along with limited modulation depth. As long as detection is in an appropriate place, there is no drift penalty in moving modulation earlier in the multiplication chain but there are interesting sensitivity effects because of the multiplier transfer slope shown in Figure 2. In one sense, a steep slope is beneficial in that the modulation depth available can be greatly increased. In another sense, this can lead to stability issues since that slope translates directly to loop gain. Thus this early modulation approach does require late stage multipliers to have modest transfer slopes.

Some of the various architectural choices relative to the classical Figure 1 are sketched in Figure 4. The level is detected from different possible locations and with various technologies and sent to a difference node after processing. After an integrator (or similar block) and other scaling/processing functions, the resultant signal drives a modulator, possibly in different locations. While different detection and modulation positions are shown as switched in the figure, only one of each may be present in a given system. Certain network analyzers and sources will employ all of the positions in different operating modes in order to optimize control range and loop performance[e.g.,10].

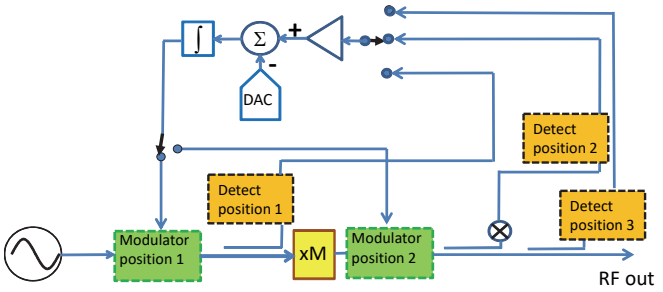

Figure 4 A number of possible leveling loop orientations are pictured in this block diagram. Different detection methods maybe be employed (diode detectors, log detectors, direct digitization, etc.).

The actual loop itself can be implemented in a number of ways. The loop could be composed entirely of analog components with which it is relatively straightforward to realize fast, tailored transient behavior. Such implementations do require care in handling wide variations in loop gain (e.g., from the multipliers) and wide control ranges will often require converting the detected signals into the log domain. The Detection blocks could be immediately digitized and another DAC could drive the modulator thus making the loop digital and, in turn, the intervening blocks could be implemented in digital hardware or in a software layer. The distinction is nuanced but the primary differences, for the purposes of this paper, are in latency and transient response time and accuracy across different time epochs.

One variation with software leveling loops involves when the leveling action is taken relative to the measurement: are they simultaneous or sequential[e.g.,11)-12)]? If the latter, then the level may be corrected at one instant and time but could be varying at the actual measurement time. Normally this would only make a difference if there was some interaction of the leveling behavior with DUT time constants. This topic will be briefly explored in section 4.

3 Loop Dynamics

For the purposes of stable control over a wide range of powers in a network analysis application, two of the primary variables of interest are control range and net transient response time. The former is normally limited by detection and modulation and examples will be covered in the next section. The latter is more often a function of the interior implementation and there are few aspects to examine.

From a practical measurement point-of-view, the transient response time can place a limit on how fast the instrument can sweep: a change in drive power due to a frequency change should ideally be settled prior to the triggering of data acquisition. The events requiring good settling response goes beyond intended frequency and power changes (as part of the sweep) to include drift of the hardware (from environmental changes, etc.) and mode changes (as may happen in a more complex setup in which the entire sweep pattern periodically changes or is shut off). On another level, changes that occur in delivered drive power to the DUT can excite time constants within the DUT (bias, thermal, and trapping, for example) which will result in a coupled net settling time for the DUT output.

To explore this concept, suppose one has a power amplifier with a relatively long time-constant bias system and it is being operated in compression where drain and gate currents are both changing substantially. If the leveling loop were to respond slowly (or have significant overshoot or other problems), the amplifier could continuously be in a complicated bias state during a power sweep measurement[11)]. Such a swept power AM/AM and AM/PM measurement set is shown in Figure 5 where two measurements were done on the same power amplifier with two different leveling systems: one relatively fast (red curve) and one relatively slow with twice the overshoot (blue curve). Even though the static power levels were within 0.1 dB, the loop dynamic differences resulted in a 0.6 dB difference in recorded 1 dB compression point (input referred) and a 1.4 degree difference in phase distortion at that compression point. The time between hardware programming (and a lock indication received) and the measurement was on the order of 10 µs.

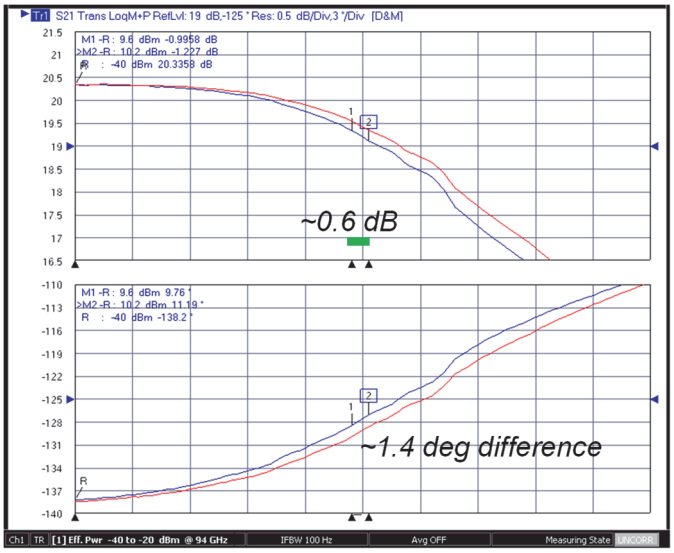

Figure 5 AM/AM and AM/PM swept power measurements of an example amplifier using two different leveling loops (red: fast; blue: slow with overshoot). The characteristics are affected by the loop dynamics.

For the analog loop implementation, the loop bandwidth is a useful metric that describes the transient response mentioned above. In a digital implementation, it is not uncommon for latency to be important: the time between when a change appears at Detection to when the resultant impact appears at Modulation. The latency arises from: ADC sampling time to achieve a desired noise level, DAC programming and settling time, and computation time for the effective integration and other processes. Of course, if this latency is large relative to the physical time constants of relevance (drift time, point-to-point sweep time, etc.), instability can result. An example of this dependence is shown in Figure 6.

A model of the loop similar to that shown in Figure 4 was simulated in time domain using Matlab's Simulink[13] with some typical loop parameters for a 110+ GHz mm-wave system. Pre-programmed patterns of power request changes (orange dots) and variations in the hardware (sweep related changes and drift; blue dots) were used in the simulation and the output power from the leveling system was monitored. Latency was then changed in subsequent runs. In the early part of the simulation one can see that the overdamped loop response to hardware changes is altered slightly with the increasing latency. Starting at about 50 µs into the time series, the power request is getting close to the maximum the system can provide so the loop stress is greater and settling time increases (even with no latency). When latency is added in this regime, instabilities start to appear as the loop can no longer correct in a timely fashion relative to the other time constants of interest. Control of this latency over all operating ranges of the loop is therefore an important design objective.

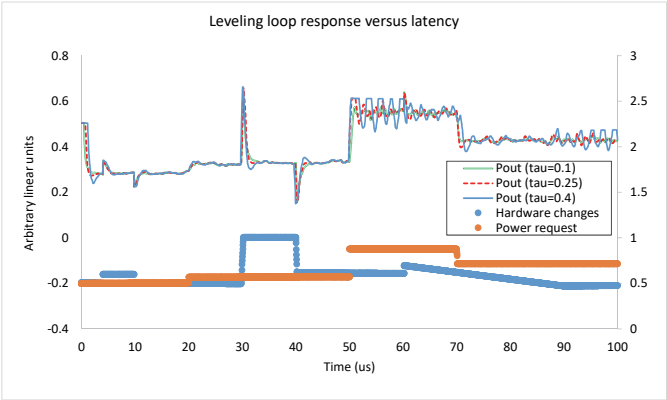

Figure 6 Leveling loop simulation where increasing latency (variable tau, in microseconds) shows a greater tendency to instability and less accurate level control.

4 Measurement results and examples

This section will illustrate some of the performance differences related to the mm-wave leveling configurations discussed in sections 2 and 3. First, consider the difference between heterodyne and (single) diode detection in a broadband 220 GHz network analyzer[10]. As discussed in section 2, the diode detection scheme will have to accommodate a rather wide noise bandwidth so the detectable control range may be reduced. Power sweeps using these two detection methods are shown in Figure 7 where the unratioed reference parameter (a3) is a proxy for output power. The curves saturate at the right of the plot as maximum power of the system is reached. The diode detection (blue curve) approach achieves about 15 dB less control range (note the plateauing at low levels) and has some added linearity deviations. The heterodyne detection scheme (red curve), based on log detection at ~12 MHz, permits the wider control range and had somewhat better thermal stability. Different diode detection circuits (e.g., multiple diodes or different technologies) may permit different results.

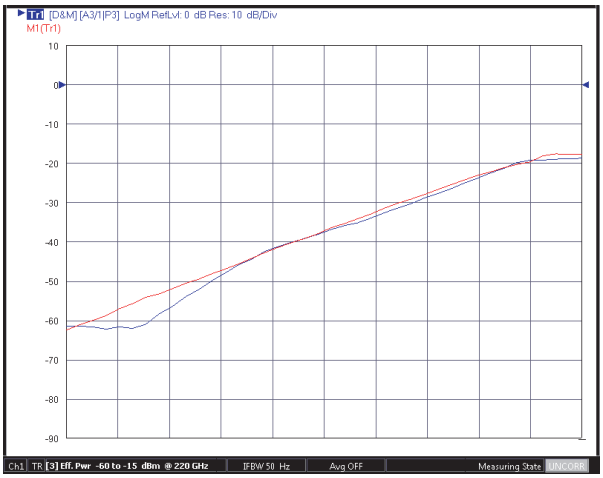

Figure 7 220 GHz power sweeps based on heterodyne detection (red curve) and direct diode detection (blue) are shown here with resulting differences in range.

Another point of comparison is based on detection before or after the later multiplication stages. While simpler from a circuit point-of-view and usually exposed to smaller noise bandwidths, the pre-multiplier detection can miss drift in the final multiplication stages and a four hour drift test was conducted to study this with a banded VNA system operating at 500 GHz. The results are shown in Figure 8 for the two different detection locations[11]. The 'pre-mult' position missed an active multiplication stage which resulted in more accuracy wander. The multiplier had a much steeper P_{out}-P_{in} slope at lower power levels which likely explains the greater error at the left part of the graph.

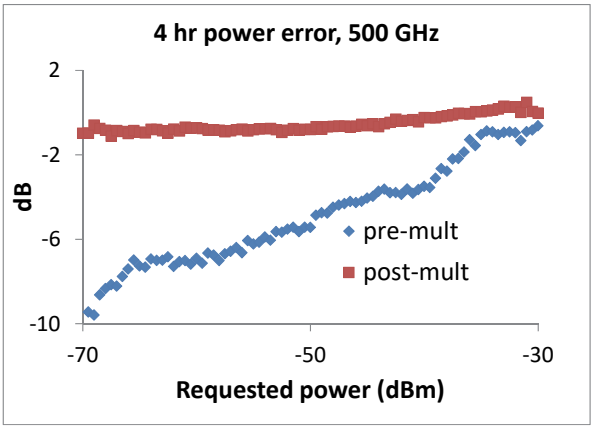

Figure 8 Detection before a final set of active multipliers resulted in more power drift over time compared to post-multiplier detection.

A final comparison is one relating to the internal loop structure: a part-time or sequential leveling approach vs. a simultaneous or real-time architecture. For this measurement, in a banded system operating at 400 GHz, the actual output power was measured by a second VNA during the extended measurement cycle of the VNA-under-test. The target power level was quite low in this case (−50 dBm) which did enhance the sensitivities since the multiplier slope was steep at this output level. As can be seen in Figure 9, the power scatter was approximately 4x higher with a part-time/sequential leveling scheme[11]. This may only be important if it leads to interactions with DUT time constants (particularly in quasi-linear measurements).

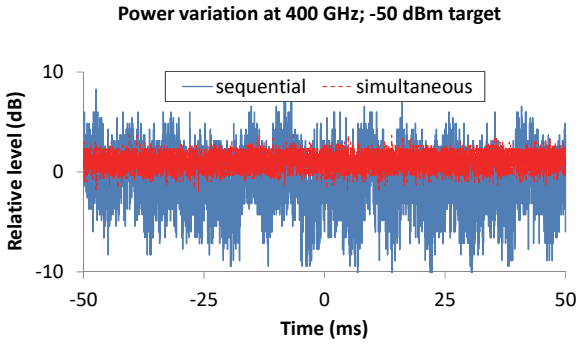

Figure 9 Leveling action sequential (part-time) with the measurement can result in more power level wander than with a simultaneous (real-time) structure.

5 Conclusions

In mm-wave network analysis, the details of how power leveling is performed can have impacts on range of power control, stability and accuracy of delivered power, and sometimes can help avoid state-altering interactions with DUT time constants. While technology and other instrument architectural considerations can affect the choices, heterodyne detection systems and low latency, real-time leveling structures can offer some performance benefits.

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