

Contribution to LTE Technology Verification - Development of MD8430A Signalling Tester

Takashi Sugimoto, Reiichi Hashimoto, Takeshi Kobayashi, Kazunori Kitagawa, Hidenori Konno, Masaki Hizume, Masato Sasaki, Katsuo Sakurai

[Summary]

LTE (Long Term Evolution) is a mobile communication system standardized by 3GPP now being deployed worldwide. We developed the MD8430A Signalling Tester to simulate LTE base stations (eNodeB) and provide a mobile terminal (UE) test environment for developing chipsets and protocols as well as for verifying performance of signals and data transfers. This tester supports key LTE technologies such as MIMO, complex MAC processing, handover and end-to-end high-speed data transmissions. Furthermore, the MD8430A supports both the TDD (same frequency channel for uplink and downlink using time division) and FDD (different frequency channels for uplink and downlink) modes.

1 Introduction

The rapid spread of smartphones and tablets terminals worldwide has caused an explosive increase in the amount of data transmitted on mobile communications networks. To solve this digital congestion, LTE (Long Term Evolution) mobile communication systems supporting large-capacity data transfer at high speeds and low latency are being deployed increasingly around the world. Anritsu has developed its new MD8430A Signalling Tester to simulate operation of LTE base stations (eNodeB) and to offer a test environment for developing chipsets and protocols used by mobile terminals (UE). This article explains the functions of the MD8430A and its implementation to achieve evaluation of key LTE technologies and performance.



Figure 1 MD8430A Signalling Tester

2 Development Concept

2.1 LTE Simulation Functions

Development of LTE chipsets and UEs requires an eNodeB simulator. The MD8430A Signalling Tester has been developed with the following concepts targeting a system configuration with the ability to respond smoothly to changes in and additions to standards.

- Use FPGA for physical layer (PHY) function to support standards changes easily as well as high-speed signal processing.
- Provide test functions for easy support of complex Medium Access Control (MAC) and Scheduling functions.
- Support MIMO test functions for new antenna technologies.
- Provide gateway function for end-to-end data communications test between UE and server.
- Provide test functions for both FDD (Frequency Division Duplex) and TDD (Time Division Duplex) technologies
- Provide GUI for analyzing communications conditions and external control interfaces for automation.

Furthermore, LTE UEs require an Inter-RAT (Radio Access Technology) function for handing over communications to W-CDMA/HSPA and GSM/GPRS cells when necessary. The MD8430A has been designed to be able to connect to and work with the MD8480C Signalling Tester targeted at

third-generation mobile communication systems to make effective use of test scenarios and support Inter-RAT tests of handovers to W-CDMA/HSPA and GSM/GPRS systems.

2.2 Achieving LTE Performance

The LTE standard 3GPP Release 8 recommendations define five categories of UE each with different maximum communications speeds. Among these five categories we targeted measurement performance for UE category 4 supporting maximum downlink and uplink speeds of 150 and 50 Mbps, respectively. To achieve this performance, the RF section must support the signal bandwidth of 20 MHz, 64QAM data modulation, and 2 x 2 MIMO operation. Since the digital section requires a performance of 10 times the communication speed for W-CDMA HSDPA (14.4 Mbps)/HSUPA (5.76 Mbps) offered by the MD8480C, it was necessary to design high-speed communications between each device, such as the FPGA and DSP, etc., as well as a large-capacity FPGA for coding processing.

3 Hardware System Design

3.1 RF Section

The RF performance related to the LTE standard specifies a signal bandwidth of 20 MHz, 64QAM data modulation, and 2 x 2 MIMO operation.

First, the digital section of the MD8430A uses a signal bandwidth of 20 MHz whereas the RF section is 100 MHz considering the need for future extendibility. Additionally, the EVM specification is 1% max to assure communications quality with a 64QAM modulation signal.

With respect to the MIMO operation, one LOCAL signal is supplied to two Tx modules to assure a fixed relative phase between the two Tx outputs.

The transmission section has a digital IF using the output of the DAC as the IF signal directly for passing to the Tx module. In theory, this method does not cause any carrier leak.

3.2 Digital Section

Figure 2 shows the block diagram of the digital section. The digital section block is not divided according to cell

functions. Instead it is divided by layer, resulting in high-speed communications between cells of the same layer. Each board has a large-capacity FPGA, supporting easy addition of extra functions. Moreover, a DSP on each board performs signal processing as well as setting of FPGA circuits, creation of log data, etc.

To assure high throughput, communications between devices are performed at high speed. Signalling between FPGAs is performed by dividing using two types of high-speed differential interface (based on clock signal and clock data recovery). In addition, communications between DSPs use a 66-MHz/32-bit PCI and Serial Rapid IO.

Although high-speed DACs are used due to the digital IF method at transmission, since sample drift may occur in sampling clock units due to FIFO in the DACs, sometimes the relative phase relationship of the four DACs may change whenever the power switch of the MD8430A is turned on. Consequently, a function for adjusting the output timing between the DACs runs at startup to align the phase relationship and assure reproducibility.

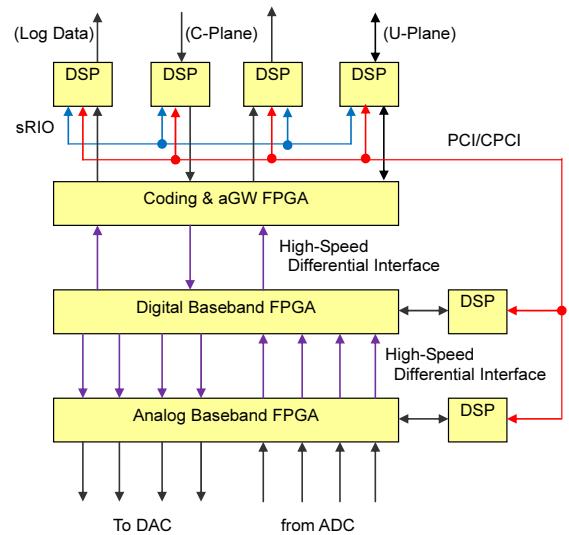


Figure 2 Block diagram of digital section

3.3 Overall System

At hardware design, several points were listed based on general considerations.

Although the signalling tester firmware version was expected to be upgraded frequently to add new standards and support customers requests, it might sometimes be down-

graded to an older version for operation comparison. The MD8430A can save a maximum of five firmware versions each of which can be switched easily in the shortest possible time.

Since several large-capacity FPGAs and high-speed DSPs are used, the cabinet design places heavy emphasis on thermal countermeasures; to maximize the effectiveness of internal air cooling, fans pull air from the front air vents directly through the cabinet and out of the back vents across the main boards arranged parallel to the flow.

Gigabit Ethernet is used for the PC/server interface because the user data transmission speed is several hundred Mbps.

A built-in CAL function improves the accuracy of the RF output level to control level changes caused by variations in ambient temperature and aging.

For ease of manufacturing and maintenance, the RF devices (relays, mux/demux) are arranged on the cabinet bottom while the boards and modules can be inserted and removed from the top. Consequently, instead of removing the RF devices from the chassis, RF modules can be installed and removed.

4 Software System Design

4.1 Software Composition

Figure 3 shows the composition of the software for the MD8430A Signalling Tester. The user specifies the scenario to execute using a GUI running on a Controller PC. The scenario executer runs the sequence described by the specified scenario and uses messages between protocols called primitives to control each layer and send and receive signalling messages. Each processing section of the MD8430A sends and receives data and controls the hardware according to the contents of the received primitives.

4.2 Performance

To achieve the required LTE performance, layer-2 processing such as Radio Link Control (RLC), MAC, etc., is partitioned to one processing section, minimizing data transfers between layers. Additionally, the downlink and

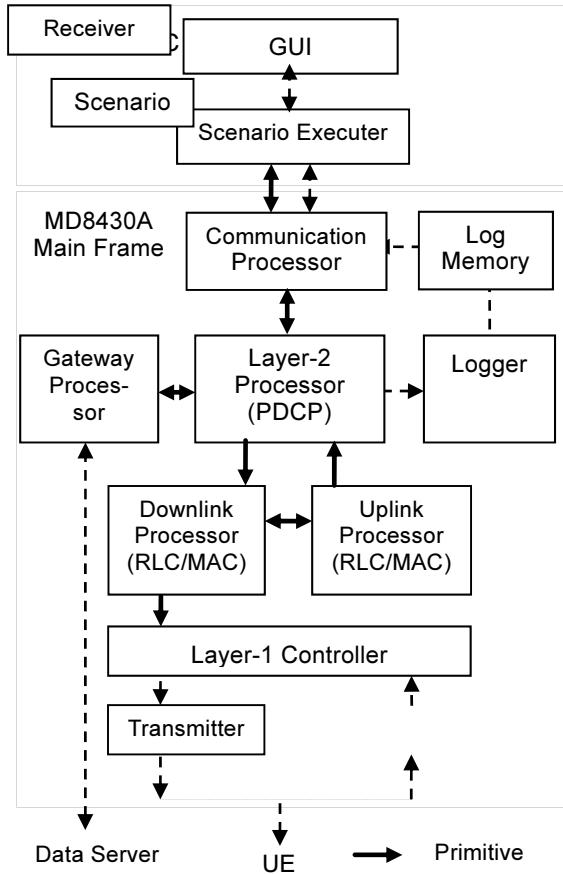


Figure 3 Block diagram of software

uplink processes are separated to allow simultaneous processing of Tx and Rx data.

The Logger receives scenario execution logs such as TRx messages and control primitives from each section for transfer to the Controller PC. To achieve the required LTE performance, Log Memory in the main frame functions as the primary storage and the system is designed to capture logs continuously at a fixed period.

4.3 Overall System

Although the MD8430A is operated mainly by the Controller PC, it has a front-panel display indicating information about the main frame and the scenario execution status. In addition, the design allows the screen to be switched by button operations for extensibility.

5 PHY Layer Processing

Key features of the LTE technology are high data throughput and low latency. The MD8430A PHY perfor-

mance supports downlink speeds of 150 Mbps, uplink speeds of 50 Mbps and processing times of 500 µs. Previous signalling testers perform basic modulation and demodulation using an FPGA and processing such as data coding/decoding, etc., in software, but the MD8430A is designed for high-speed processing, so almost all PHY processing, including data coding/decoding, is performed using FPGAs. Moreover, not only does the MD8430A support chipset verification and protocol testing but it also has the necessary support such as 6-cell signal simulation for system configurations used at 3GPP tests, such as conformance tests. Additionally, conventional testers were configured to process each cell in each hardware unit and such configuration was a barrier to performing Inter-Cell Handover tests. To overcome this problem, the MD8430A executes processing for multiple cells using the same hardware unit. As a result, the MD8430A FPGA is designed to deal with two problems: minimizing processing time, and miniaturizing circuits. The FPGA processing is pipelined and parallel to greatly reduce processing wait times as well as processing time itself. Due to the excellent, high-performance circuit design, multiple cell signals can be processed by time-sharing in one circuit, helping circuit miniaturization. However, since many parts of the standards were undecided during the MD8430A development, there was a high possibility of design changes during the development stage to meet the various test needs of leading customers worldwide. Consequently, each processing function was designed as an independent block and the overall controller was moved out of the blocks. As a result, even if individual blocks changed, the function changes could be easily accommodated simply by adjusting the controller. Figure 4 shows the composition of the LTE basic PHY layer processing function.

6 MAC Layer Processing

The MAC processing section has built-in a MAC function meeting the 3GPP TS36.321 standard. Figure 5 shows the MAC processing structure. The MAC processor supports the following main functions:

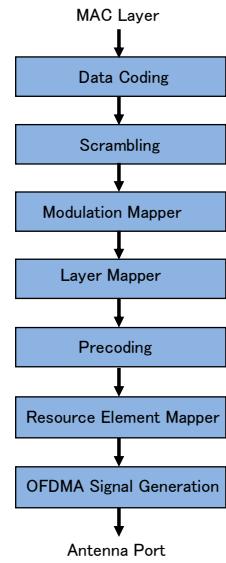


Figure 4 LTE Physical Layer Processing

- Mapping between logical channel and transport channel
- Mux/Demux
- HARQ (Hybrid Automatic Repeat Request)
- Scheduler
- Random Access

In addition to the HARQ operation, the HARQ processor has a function for reversing the CRC bit for DL-SCH settings and setting UCI HARQ-ACK data; it can be used to intentionally perform resend processing.

The Scheduler has a function for setting MCS, RB, and subframe scheduling. In addition, it can use Channel information (CQI, PMI, RI) from the UE for various schedules and allocations by setting parameters such as MCS, etc.

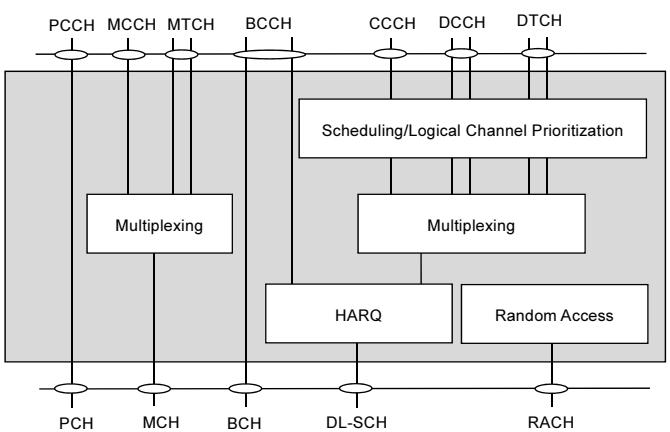


Figure 5 Outline of MAC structure

The Random Access Procedure is composed of three statuses:

1. From RA Preamble reception to RA Response transmission
2. From UL-SCH (Msg3) reception to Contention Resolution transmission
3. From Contention Resolution confirm to RA Procedure processing completion (Reconfiguration, RRC procedure delay).

The transition to each status depends on the data reception regarded as the transition condition and the type of Random Access Procedure working as the trigger.

To support the transition to each of these statuses, the operation from each status is predefined (macro definition function), and the defined operation is triggered by a specific event.

Moreover, different macros can be defined for multiple actions for one event. As a result, it is possible to execute the abnormal and normal RA Procedure test alternately for the RA Preamble reception for example.

In the LTE standards there are five types of Contention-based Random Access Procedure as follows:

- Initial access from RRC_IDLE
- RRC Connection Re-establishment procedure
- Handover
- DL Data arrival
- UL Data arrival

There are also two types of non-contention based random access procedures as follows:

- Handover
- DL Data arrival

for a total of seven defined types of Random Access Procedures. All Random Access Procedures can be tested by a combination of macro definitions.

7 MIMO Test Function

7.1 DL-MIMO Signal Transmission

The MD8430A downlink signal generation circuit uses two Tx antennas per cell and can generate a downlink sig-

nal for six cells (Cell #1 to Cell #6). However, Cell #1 is configured for use in combination with the Tx antennas used by Cell #2 so it can use four antennas.

In other words, although up to 12 antennas can be used at the cell side, the number of Tx RF units is configured in principle to provide signals for the UE Rx antennas [UE Rx antenna count x Frequency channels]. Since the actual number of UE Rx antennas is two and the number of frequency channels is two, the total number of Tx RF units is four.

Since the MD8430A simulates the UE Rx antenna signal at the Tx RF output, the baseband signal processor placed at the previous processing stage of the Tx RF unit is configured to execute propagation path modelling.

Either the simple propagation path function built into the MD8430A or the Anritsu MF6900A Fading Simulator can be used as the propagation path modelling method.

7.2 MIMO Function Test using Simple Propagation Path

The propagation path model built into the MD8430A can be set to static and one-path-per-channel 2 x 2 or 4 x 2 propagation path. For example, when configuring a 2 x 2 propagation path, the propagation path characteristics can be set as a 2 x 2 matrix composed of four complex elements.

The simple propagation path can be used to confirm whether or not the UE has reported appropriate feedback information corresponding to changes in the propagation path characteristics.

For example, when setting the 2 x 2 propagation path H shown below, it is possible to confirm whether or not the RI (Rank Indicator) reported by the UE becomes the expected contents.

$$\text{Rank}=2 : H = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \quad \text{Rank}=1 : H = \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$$

In addition, it is possible to confirm whether or not the PMI (Precoding Matrix Indicator) reported by the UE becomes the appropriate value for the set propagation path. For example, when executing 1-layer closed-loop spatial multiplexing with two Tx antennas on a cell, the UE specifies any of the following four vectors using the PMI.

$$F_0 = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ 1 \end{bmatrix}, F_1 = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ -1 \end{bmatrix}, F_2 = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ j \end{bmatrix}, F_3 = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 \\ -j \end{bmatrix}$$

As an example, when setting propagation path H_x calculated by the following equation as a simple propagation path, PMI reported by the UE should specify F_x as the precoding vector. Here, F_x^H denotes the transposed complex conjugate of F_x .

$$H_x = F_x \cdot F_x^H$$

7.3 MIMO Performance Test using MF6900A

Using the Anritsu MF6900A Fading Simulator it is possible to support 2 x 2 and 4 x 2 multipath fading propagation models defined by the 3GPP measurement standards.

The downlink signal for each cell generated by the MD8430A is handed from the MD8430A to the MF6900A and, after application of the fading effect, returned to the MD8430A for output from the Tx RF unit.

7.4 DL-MIMO Connection Test

The MD8430A supports each of the 3GPP downlink Tx modes for performing connection tests using MIMO propagation paths, such as Open/Closed-loop Spatial Multiplexing, Transmit Diversity, and MU-MIMO.

In an MU-MIMO test, the data on the PDSCH for the test UE can be multiplexed on the same RF resource with the PN data on the PDSCH for another assumed UE.

At this time, the precoding vector specified by the UE via the PMI is used for sending the PDSCH to the test UE. On the other hand, the precoding vector for sending the PDSCH to the other UE is automatically selected so that it shall be orthogonal to the precoding vector for the test UE.

7.5 UL Tx Antenna Selection

Until 3GPP Release 9, the LTE standards specifies Tx antenna selection as the only function for using multiple Tx antennas to transmit the uplink signal. The MD8430A can monitor which of the two UE Tx antennas is being used to send the signal.

8 Data Communications Test Function

The MD8430A is connected to an external data server via the Server Port to execute the packet data communications test. The input IP data is transferred to lower layers via the Gateway processor and PDCP (Packet Data Convergence Protocol) layer.

8.1 Gateway Processing Section

The Gateway processor has functions equivalent to the Serving Gateway and PDN Gateway standardized by 3GPP TS23.401. The functions, such as TFT Filtering, Prefix Advertisement, DHCP Server, etc., are set by specifying parameters from scenarios. These functions can be used to make detailed settings such as management of the data transmission path, notification of network data to the UE, allocation of the UE IP address, etc., for configuration of a complicated test environment such as Multiple PDN.

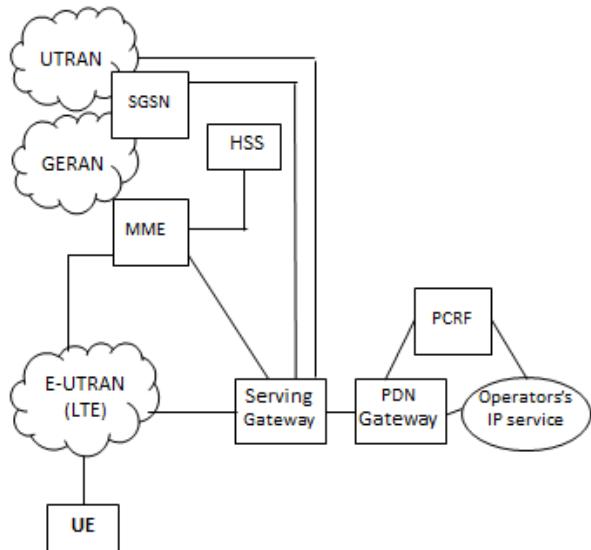


Figure 6 LTE Network architecture

8.2 PDCP Layer

The PDCP processor has 3GPP TS36.323 functions such as ROHC (Robust Header Compression), Ciphersing, Integrity, etc., and can be used for tests in environments with compressed transmitted packet header data, and ciphersing/authentication. The ROHC function supports the following profiles for testing various protocol packets.

- No compression (0x0000, RFC3095)

- RTP/UDP/IP (0x0001, RFC3095)
- UDP/IP (0x0002, RFC3095)
- ESP/IP (0x0003, RFC3095)
- IP Only (0x0004, RFC3843)

9 TDD Test Function

Both the LTE FDD and TDD technologies are supported by the MD8430A. The TDD technology shares the same frequency channel for both uplink and downlink and performs communication using time division, offering a variety of advantages. First, because the same frequency is used for uplink and downlink, it has the advantage of making good use of available frequencies compared to FDD. Figure 7 shows an example of the TDD frame structure. The TDD signal frame is composed of subframes for downlink data, subframes for uplink data, and a special subframe including DwPTS/UpPTS/GP. The Guard Period (GP) is a signal gap for preventing interference between the downlink and uplink signals.

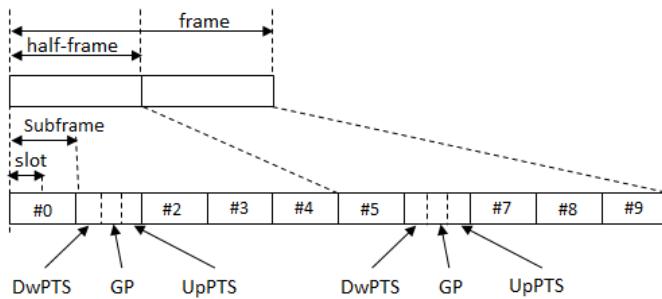


Figure 7 Example of TDD frame structure

Second, since it is possible to perform asymmetric uplink and downlink settings at the same frequency, it has the advantage of changing the uplink and downlink communications capacity. The MD8430A supports Uplink–Downlink Configurations (Table 1) as the parameters for setting the uplink and downlink communications capacity.

Table 1 Uplink–downlink configurations

| Uplink-downlink configuration | Subframe number | | | | | | | | | |
|-------------------------------|-----------------|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | D | S | U | U | U | D | S | U | U | U |
| 1 | D | S | U | U | D | D | S | U | U | D |
| 2 | D | S | U | D | D | D | S | U | D | D |
| 3 | D | S | U | U | U | D | D | D | D | D |
| 4 | D | S | U | U | D | D | D | D | D | D |
| 5 | D | S | U | D | D | D | D | D | D | D |
| 6 | D | S | U | U | U | D | S | U | U | D |

D: Downlink, U: Uplink, S: Special subframe

In addition, since the same frequency is used for uplink and downlink, beamforming for collecting the signal power from the eNode and targeting it at the UE is relatively easy compared to FDD. Beamforming improves reception conditions and should improve the data throughput performance. The MD8430A can simulate the Beamforming Model specified in the 3GPP TS 36.521-1.

10 User Interface

The MD8430A is controlled by the MX843010A Control Software running on an external PC. The control software executes C programs (called scenarios) describing the signalling tester simulation operations, and displays and analyzes the execution results.

10.1 Data Display and Analysis

Data passing between the control software and MD8430A as well as between layers within the MD8430A is appended with header information describing the send source and destination, transmission timing, etc., and is managed as a single unit called a primitive. The user can confirm the primitive communications records (trace log) and can obtain the results of the simulation described by the scenario. Since the primitive displays the analysis in real time in the trace log, the user can immediately understand the control results. Control data such as DCI and UCI is sent and received between the eNodeB and UE. After the trace log has been saved, the contents of the control data can be easily grasped by running the Trace Converter application to

convert the log to a csv file format. The Trace Converter application can be used to analyze the Header, Control Element, and Random Access Response in the MAC PDU.

10.2 GUI-based Analysis Support

With respect to the user data channel, the TRx data counts, transmission speeds, etc., in each layer can be counted and displayed. In addition, these measured data are displayed as graphs so conditions can be monitored visually. Figure 8 shows an example of a graph of the user data TRx speeds.

10.3 Automated Testing using SS Interface

The control software is operated via the built-in SS Interface (SS: System Simulator) using C programs created by the user. The user uses created programs using this interface to automate test operations such as starting/stopping the control software, executing the selected scenario, saving log files, etc.



Figure 8 Graphical display of user data transmission speed

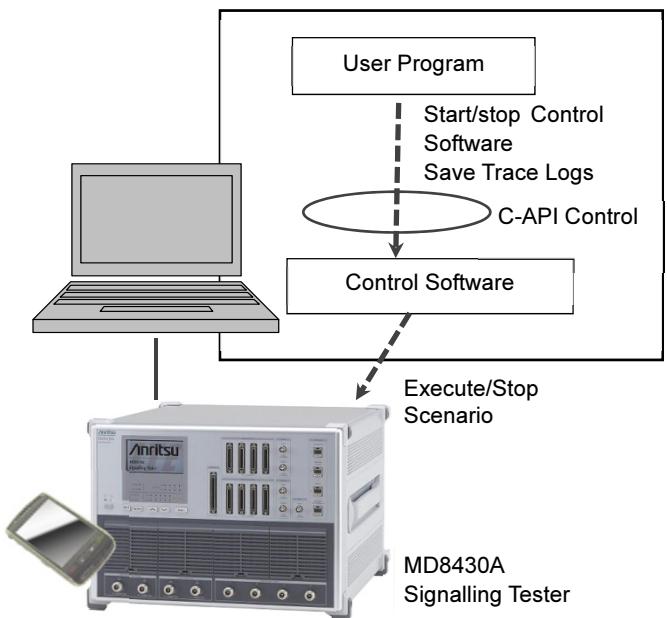


Figure 9 Test automation using user program

11 W-CDMA/HSPA, GSM/GPRS Inter-RAT Test

The MD8480C Signalling Tester for the 3rd generation mobile communications has been widely used for development of W-CDMA/HSPA UEs and UE chipsets. The MD8430A has an interface for connection with the MD8480C as well as functions for relaying control data from the Controller PC and user data from the data server to the MD8480C. Using these functions, both of the LTE operation simulated on the MD8430A and the operation of W-CDMA/HSPA and GSM/GPRA simulated on the MD8480C can be performed in a collaborative manner. With these functions, it is possible to perform the required system switching and handover tests as the UE moves from an LTE service area to W-CDMA/HSPA and GSM/GPRA service areas.

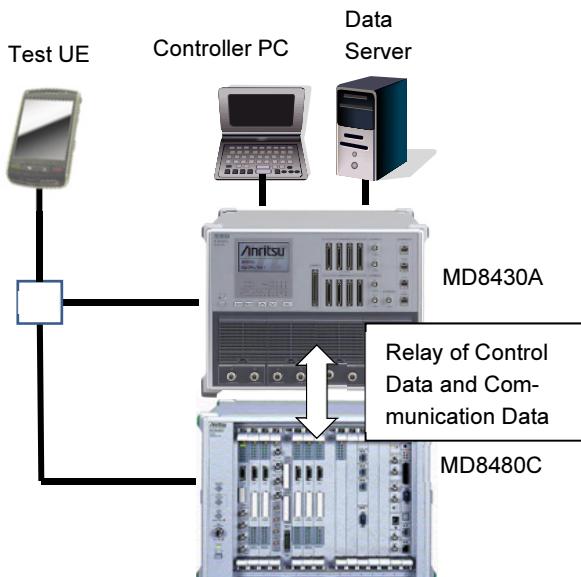


Figure 10 Inter-RAT test system configuration

12 Summary

We have developed the MD8430A Signalling Tester for development of LTE UE chipsets and protocols supporting large-data-capacity, high-speed, and low-latency next-generation mobile communications. The MD8430A has been adopted by the world's main chipset and terminal vendors as an essential test tool for verification of LTE technologies requiring complicated signal processing and high performance. In addition, it can be used as a key system component for conformance tests and carrier acceptance inspections to improve the quality of LTE services. The LTE standard is being continuously revised to support increasingly faster data transmission speeds and larger network capacity and Anritsu is continuing to support the industry with test solutions for verifying future new technologies.

Authors



Takashi Sugimoto
2nd Product Development Dep.
R&D Div.



Reiichi Hashimoto
2nd Product Development Dep.
R&D Div.



Takeshi Kobayashi
2nd Product Development Dep.
R&D Div.



Kazunori Kitagawa
2nd Product Development Dep.
R&D Div.



Hidenori Konno
2nd Product Development Dep.
R&D Div.



Masaki Hizume
2nd Product Development Dep.
R&D Div.



Masato Sasaki
2nd Product Development Dep.
R&D Div.



Katsuo Sakurai
2nd Product Development Dep.
R&D Div.

Publicly available