Development of 32 Gbit/s Pulse Pattern Generator / Error Detector

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[Summary] With the increasing demand for cloud computing and high-definition video streaming, storage and server transfer speeds are increasing, and the transmission capacities of core communications networks are also increasing rapidly too. To meet these trends, the transfer speeds of physical-layer devices and modules are increasing and signal quality analysis is becoming more important in assuring service quality. The MU18302xA/MU18304xA 32 Gbit/s Pulse Pattern Generator/Error Detector support the multichannel simultaneous BER measurements and crosstalk tests required for development of PC boards and devices targeting ultra-high-speed interconnects up to 32.1 Gbit/s for even more accurate ideal signal quality analysis.

1 Introduction

The rapid recent market growth of cloud computing, smartphones and LTE services has led to speed bottlenecks at internal interconnects in high-end servers and storage devices in data centers. Solving these bottlenecks has led to increasing adoption of revolutionary high-bit-rate, multi-lane internal interconnect technologies, such as Fibre Channel, InfiniBand, PCIe, Serial Attached SCSI (SAS), etc., supporting high speeds, high density and low power consumption.

In addition, the long-haul communications market is also seeing active development in digital coherence as a large-capacity transfer technology following on from higher bit rates and WDM, multiplexing, and next-generation optical devices and modules supporting 40/100G carrier networks. This in turn is increasing demand for high-bit-rate multichannel measuring instruments.

Anritsu has released its MP1800A Signal Quality Analyzer (SQA) to support new market demand for a wide range of measurements targeting quality evaluation and management of optical modules and high-speed devices. This all-in-one SQA uses plug-in modules to support measurement of up to 8 channels at maximum bit rate of 32.1 Gbit/s. Two new options have been developed for it: the MU183020A/21A 32 Gbit/s Pulse Pattern Generator (32G PPG) and the MU183040A/41A 32 Gbit/s Error Detector (32G ED). To support high-accuracy jitter tolerance tests and signal quality analysis up to 32.1 Gbit/s, the 32G PPG can operate in conjunction with the MU181500B Jitter Modulation Source to add Sinusoidal Jitter (SJ), Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), and Spread Spectrum Clock (SSC), simultaneously, as well as with the MP1825B 4Tap Emphasis (Emphasis) for correcting attenuation of high-speed signals to assure an open Eye waveform. This article describes the development concept, system design, main performance, and typical measurement applications of the 32G PPG and 32G ED.

2 Development Concept

Development of a high-bit-rate, multichannel, low-cost, all-in-one SQA was based on the following concepts:

- High Bit Rates
  Present-day applications require bit rates up to 28 Gbit/s per lane for 100 GbE devices, but we aimed to support rates up to 32.1 Gbit/s for 100G long-haul transmissions, considering future applications.
- Multichannels
  Evaluation of interconnects requires a 32G PPG for synchronization of up to 8 channels and the development goal was to combine the 32G PPG and ED to achieve simultaneous installation of a 4-channel 32G PPG and ED in one main-frame cabinet.
- Low Cost
  The goal was to simplify the circuits and automate adjustment, thereby halving the cost in comparison to a 28-Gbit/s configuration using existing SQA 14G PPG/ED modules.
- All-in-One Design
  The SQA is designed with six slots to accommodate plug-in modules. As a result, in addition to multichannel measurement, it can be configured freely for various measurement applications by adding modules with other functions under linked and automated control.

3 System Design

3.1 Blocks

Figure 1 shows the basic structure of the 32G PPG. The data processing direction of the 32G ED is just the reverse of the 32G PPG and the basic structure is unchanged. Both the 32G PPG and 32G ED have a large-capacity FPGA to perform separate dual-channel logic processing and support easy addition of extra functions. The size has been reduced by using a soft-core CPU in the FPGA and integrating the Ethernet communications interface with the SQA main frame.

Operation of the clock controller has been simplified by automating generation of the multiplier and division clocks required for internal data processing according to the input frequency.

The RF Block uses a newly developed high-frequency module package to assure high output waveform quality and high accuracy.

The multi-sync controller synchronizes modules to support the multiple channels as explained in the next section.

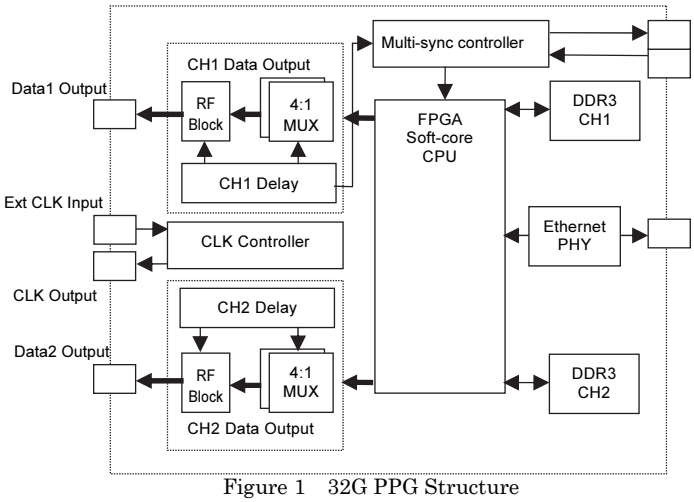

Figure 1 32G PPG Structure

3.2 Multichannel Support

The Active Optical Cable (AOC) used by the Infiniband standard supports 8 channels of 4 channels in each direction and the next-generation CFP2/4 module uses 100-GbE four-channel signalling. In these types of applications using multi-lane configurations, extra consideration must be given to assuring skew tolerance and resistance to crosstalk effects.

Since the 32G PPG uses multiple plug-in modules to support various applications using multiple lanes, it has a Combination function for generating and receiving linked multichannel patterns (Figure 2), as well as a channel synchronization function for arranging the pattern generation timing of multiple channels (Figure 3).

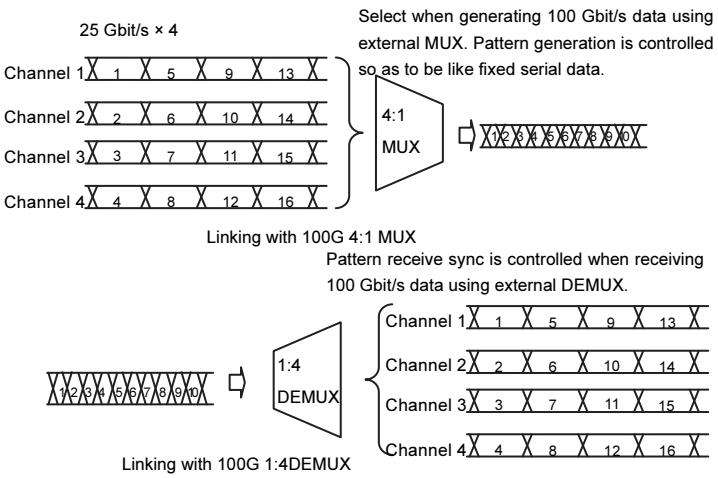

Figure 2 Combination Pattern Generation/Reception

The channel synchronization function (Figure 3) can arrange the data pattern generation timing for up to 8 channels.

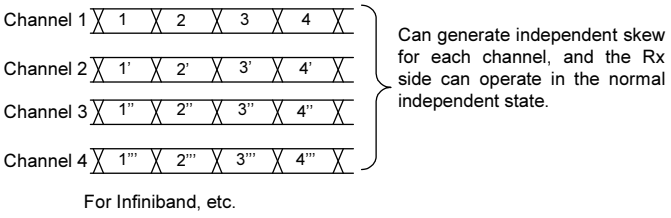

Figure 3 Channel Synchronization Pattern Generation

Figure 4 shows the multichannel block diagram of the 32G PPG. The 32G PPG composed of 2 channels performs multiplexing at the FPGA and MUX using the internal divided clock to generate the data. Using the common clock, two channels are output from the FPGA, and the phases of divided clocks from two 8:2 MUXes are detected by the Phase Detector (PD) to match the clock phases.

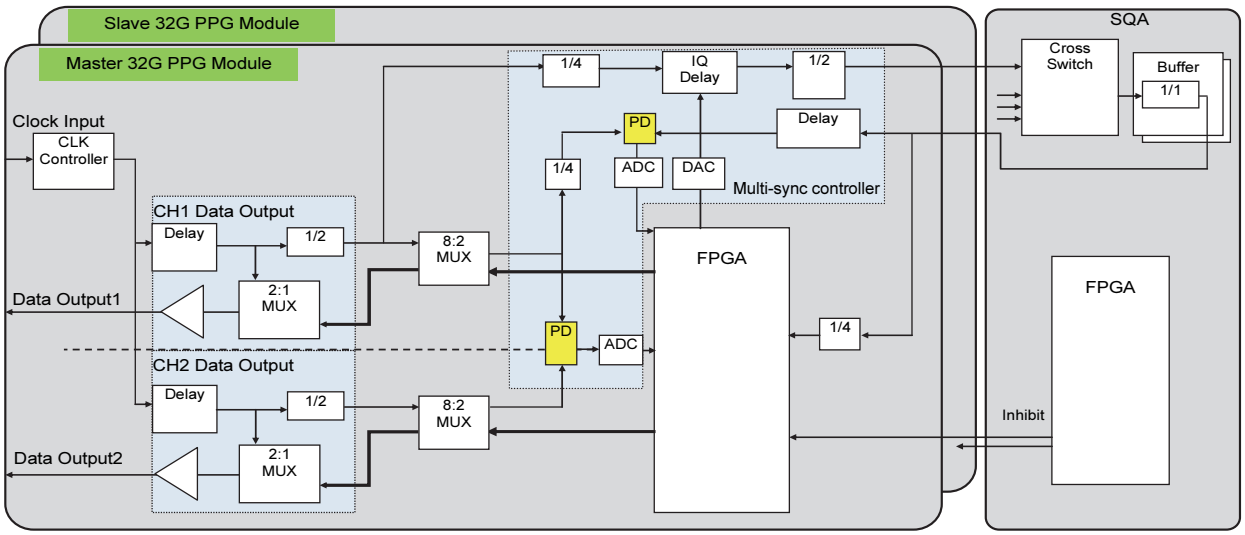

Figure 4 32G PPG Multichannel Block Diagram

Synchronization between different Master and Slave mod-ules uses the SQA main frame Cross Switch to distribute the 32G PPG frequency division clock to all modules. The PD detects the phase of the module internal clock and the distributed clock while the Slave 32G PPG uses software-based monitoring to control the clock divider so that the voltage is the same as the Master voltage; multichannel control is done by aligning the data generation permutations and matching the internal clock frequency division timing of each module.

3.3 Size and Power Reduction

As shown in Figure 5, the current 28 Gbit/s PPG and ED con-figurations achieve 28 Gbit/s by combining two 14G PPG or ED modules to perform MUX/DEMUX. As a result, a total of six slots is required for 2-channel 28 Gbit/s. The configu-ration described below requires 1/6 of the space of current modules and 1/4 of the power.

- One FPGA handles the data processing and MUX/DEMUX now handled by separate modules.
- Integration of Filter Bank required by electronic delay into 1/4 the previous size.
- Integration of RF circuits (MUX, DEMUX, Limiting Amp, etc.) using InP HBT process semiconductor.

By using these techniques, PPG/ED modules can be installed to support up to 8ch in main frame, and a jitter modulation source has been incorporated in the main frame too, expanding support for future applications.

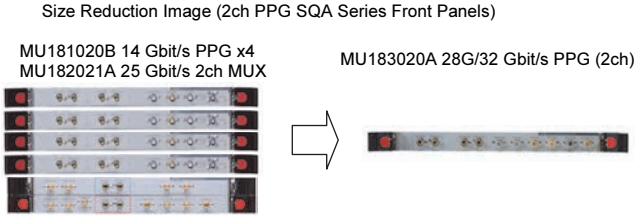

Figure 5 Comparison with Current Modules

4 Main Hardware Performance

4.1 Low-Jitter, High-Quality Waveforms

The 32G PPG can output signals up to 3.5 Vp-p (single end) to match the measurement application and depending on the selected output option. In addition, since the cross point can be controlled from 20% to 80%, Electro-absorption Modulator Integrated Laser (EML) and phase modulators can be driven directly.

As shown in Figure 6, the output data waveform has low waveform distortion with intrinsic jitter of less than 500 fs rms (true value) at 32.1 Gbit/s. This performance is achieved by using a MUX IC[1]) (Figure 7) and Limiting Amp using a newly developed InP HBT process, supporting high-frequency modules. Single InP HBT process transistors offer superior high-speed performance with a maximum oscillation frequency of 479 GHz and cutoff frequency of 233 GHz. Both an output amplitude of 540 mVp-p and a wide Eye opening are achieved at 100-Gbit/s operation by using a MUX IC manufactured using this process. Figure 8 shows the waveform at 100-Gbit/s operation. The low-jitter waveform is achieved by assuring sufficient operation margin at 32.1-Gbit/s operation. As a result of the low-jitter

PPG output, combination with a jitter modulation source supports high-accuracy jitter tolerance tests by addition of minute amounts of jitter.

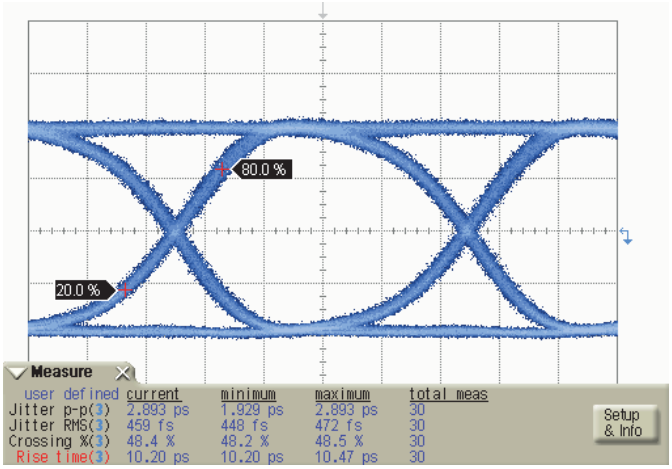

Figure 6 32G PPG 32.1 Gbit/s 3.5 Vp-p Waveform

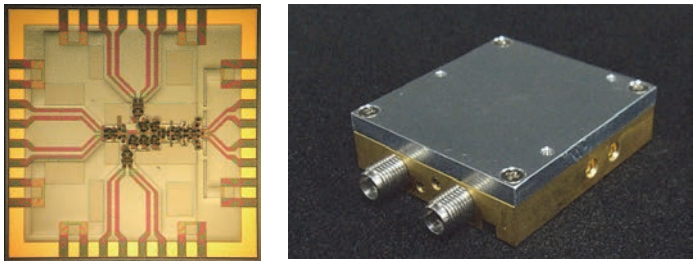

Figure 7 2:1 MUX Chip and RF Module

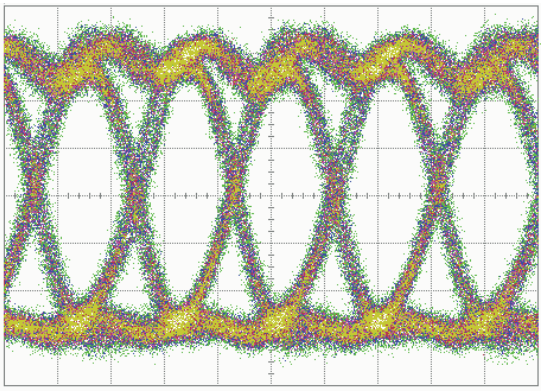

Figure 8 2:1 MUX 100 Gbit/s Waveform (5 ps/div, 100 mV/div)

4.2 High Input Sensitivity and Wide Phase Margin

As a result of the high-sensitivity input performance, the 32G ED can measure low-amplitude signals with high accuracy. Like the 32G PPG, the 32G ED uses the same newly developed InP HBT process Limiting Amp and DEMUX IC to achieve small module packages with an input sensitivity of better than 50 mVp-p at 32.1 Gbit/s (Figure 9), and a phase margin of better than 690 mUI (true value at 32G PPG/ED loopback). Additionally, the threshold voltage and phase of the data signal input to the 32G ED can be detected to support an auto-adjust function for tracking the threshold voltage and phase settings to consistently minimize error rate. The result is long-term stable BER measurement even when the input signal phase and input data offset are changing due to ambient temperature variation.

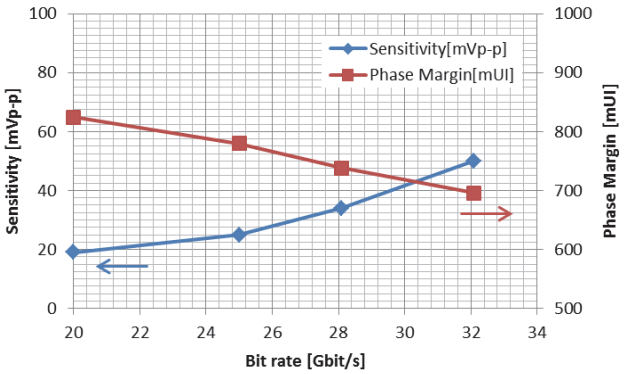

Figure 9 32G ED Input Sensitivity and Phase Margin

4.3 Variable Phase Circuits with High Linearity

The phase shifter (delay incorporated into Data out of Figure 4) has high linearity. The phase shifter uses an IQ modulation method first developed for the SQA. A characteristic of the IQ modulator is that the phase can be varied at any cycle independent of frequency, offering the great advantage of smaller size compared to mechanical phase tuners.

Figure 10 shows the phase tuner block diagram. In this circuit, the clock is 1/32 frequency divided before and after the IQ modulator. These frequency divided clocks are phase compared at EXOR and the output voltages are detected by the ADC. The high linearity phase control is achieved by feedback to the IQ modulator according to the detected voltage.

Figure 11 shows the linearity of the phase setting. The phase setting range is –1000 to +1000 mUI; since the linearity error is less than 25 mUI (true value) at a setting of 1000 mUI, both the phase margin and Bathtub/jitter characteristics can be measured with very high accuracy. Furthermore, the phase error of multiple signals can also be measured because the phase tuner can be controlled independently for each channel.

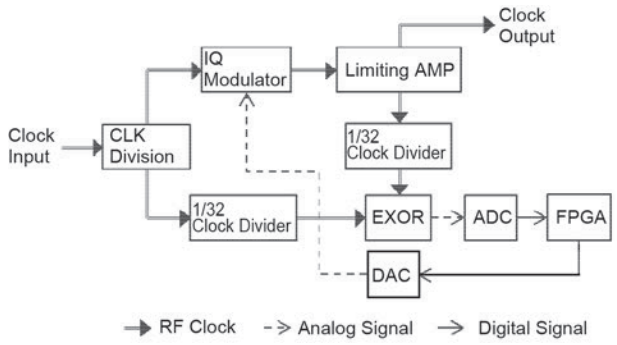

Figure 10 Phase Shifter Block Diagram

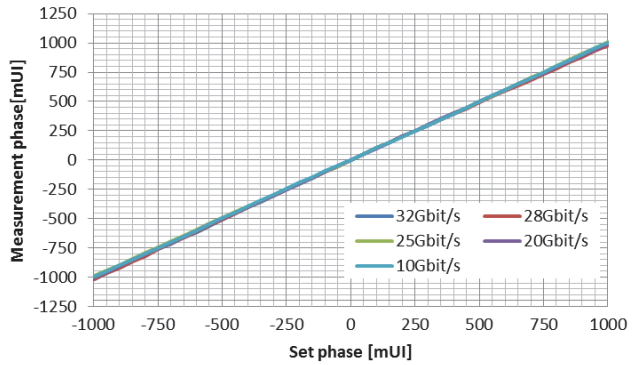

Figure 11 Phase Shifter Characteristics

5 Software System Design

5.1 Software Blocks

The SQA series is composed of a hardware mainframe to which plug-in modules are added. Consequently, the software structure is independent of each module. However, the Combination and Tracking functions (section 5.4) to control other modules operate via a common section.

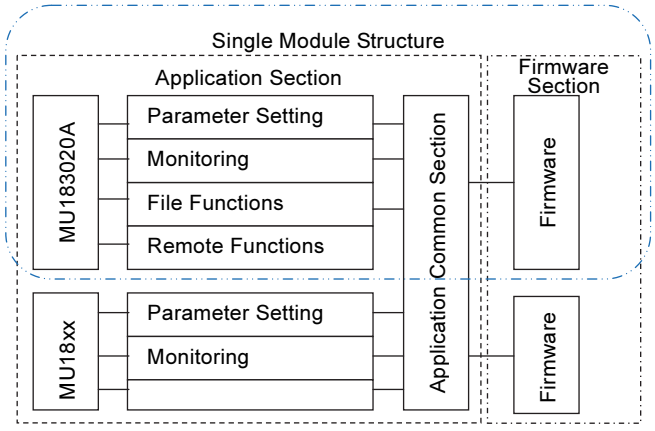

Figure 12 Software Block Diagram

Figure 12 shows the software overall block diagram. Each software module is composed of an application section for setting parameters using a GUI, displaying results, and performing remote control, plus a firmware section for controlling hardware.

5.2 Backwards Compatibility

Since each screen for setting the 32G PPG/ED parameters and displaying the results shows the same images as the 14G PPG/ED modules for the SQA series and inherits the same operability, users easily understand the operations based on previous experience. Similarly, the remote commands are also backwards compatible with the earlier 14G PPG/ED, allowing users to re-use previously created programs with few modifications.

5.3 Multichannel Results Display

The MU183040A has interfaces for two data channels, while the MU183041A supports four data channels. The BER measurement results can be displayed simultaneously for each of channels 1 to 4. Figure 13 shows an example of BER measurement results for four channels. Consequently, simultaneous multichannel measurement results can be understood at a glance. When measuring serial data bit error rates of two or four channels carrying 32 Gbit/s data per channel simultaneously, the Combination function supports both display of the total results for the serial data for all channels (left screen in Figure 13) and for each channel (right screen in Figure 13).

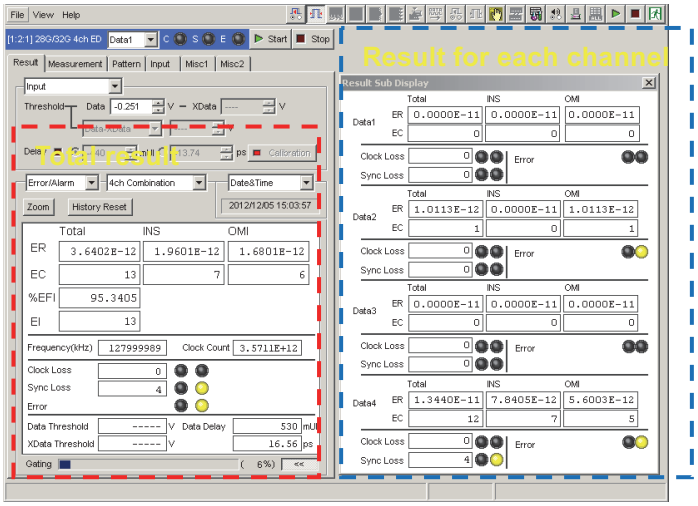

Figure 13 BER Measurement Results

5.4 Tracking Synthesizer and Jitter Modulation Source Modules

The 32G PPG can track the operation of the SQA series MU181000A/B Synthesizer and Jitter Modulation Source modules. When tracking the synthesizer, the bit rate can be set from the 32G PPG setting screen. Additionally, when tracking the jitter modulation source, SJ/RJ/BUJ jitter can be impressed on the data output according to the 32G PPG output bit rate.

Figure 14 shows the bit rate setting and data flow when the 32G PPG and synthesizer are tracking. Setting across multiple modules is performed via the Application Common Section.

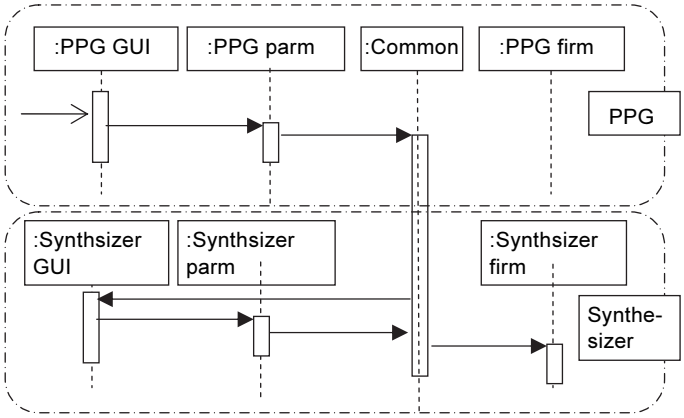

Figure 14 32G PPG and Synthesizer Data Tracking

6 Measurement Application Examples

Starting with communications technologies standardized by IEEE802.3ba, data transmission speeds exceeding 100 Gbit/s are being developed and achieved using multichannel signals. As described in sections 3 and 4, the multi-channel system and the phase shifter circuit of the 32G PPG/ED support high-accuracy evaluations.

6.1 Evaluation of 100 GbE Optical Module

Figure 15 shows an example of 28 Gbit/s x 4 CFP2 evaluation. Using a 4ch 32G PPG/ED supports evaluation of next-generation communications optical modules such as CFP2. Optical modules are becoming increasingly smaller and more integrated, making both jitter and input sensitivity tests as well as crosstalk tests between channels especially important. With synchronizing between four channels as well as independent pattern and phase setting functions, the 32G PPG/ED easily supports evaluation of individual channel performance and cross-channel effects.

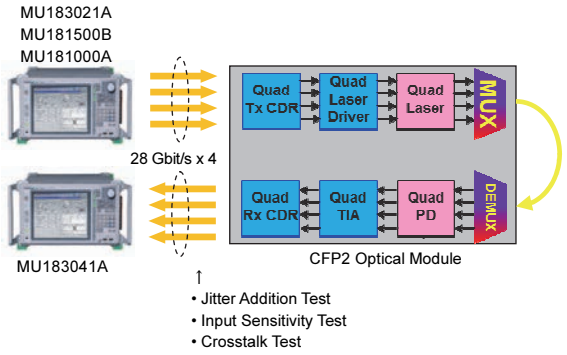

Figure 15 CFP2 Optical Modulator Evaluation

6.2 AOC Evaluation

The MU183021A channel synchronization function is ideal for duplex evaluation of AOCs used in high-speed interfaces such as Infiniband.

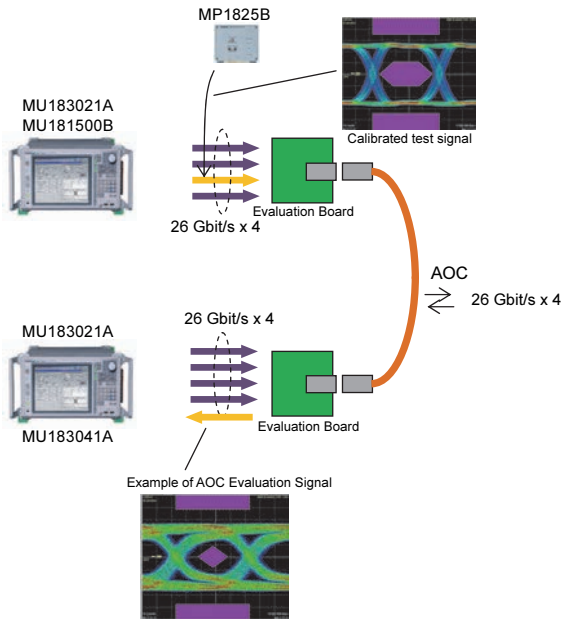

Figure 16 AOC Evaluation

Figure 16 shows an example of 26 Gbit/s x 4 AOC evaluation. Combining the Jitter Modulation Source and Emphasis supports calibration of signal quality according to the test standards and evaluation of transmission characteristics, including crosstalk effects in both directions. In this test, a 26 Gbit/s x 4 signal is input in both directions and the characteristics after passage through the AOC are evaluated using one of these signals after calibration. Adding jitter using the Jitter Modulation Source and controlling the transmission loss using the Emphasis support more accurate measurements of the performance margins of devices.

7 Summary

The 32G PPG/ED has been developed to support R&D into next-generation optical modules and devices for high-bit-rate multichannel applications. Combining the various plug-in modules for the SQA series enables quality analyses of 8 signal channels at speeds up to 32.1 Gbit/s for a variety of applications.

As the optimum measurement solution for multichannel, ultra-high-speed signal, and jitter evaluation, the 32G PPG/ED both cuts evaluation times and increases evaluation quality for today's ever-more complex high-speed devices and modules.

References

1) Y. Arayashiki, Y. Ohkubo, T. Matsumoto, Y. Amano, A. Takagi, Y. Matsuoka: "A 120-Gbit/s 1.27-W 520-mVpp 2:1 Multiplexer IC Using Self-Aligned InP/InGaAs/InP DHBTs with Emitter Mesa Passivation" IEICE TRANS. ELECTRON., Vol. E93, No. 8, 2010.

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