Development of MD8480C Supporting HSPA Evolution

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[Summary] The mobile communications market is transitioning to the LTE (Long Term Evolution) wireless standard. However, many carriers are upgrading existing UMTS equipment by using W-CDMA HSPA Evolution. The MD8480C simulates a UMTS base station and provides tests, such as mobile terminal (UE) encoding/decoding, voice calls, data communications (call switching, packet), and MS-to-MS, for development of UE chipsets and protocols. The MD8480C supports HSPA Evolution in Release7 and 8, such as 64QAM, MIMO, and DC-HSDPA.

1 Introduction

The rapid spread of mobile-terminal data devices represented by modern smartphones is causing an explosive increase in network data volumes. The 3GPP Long Term Evolution (LTE) standard was developed to solve this problem and is currently being deployed in countries like N. America, S. Korea, Japan, etc. However, supporting LTE requires base station hardware upgrades, in turn requiring heavy capital investment for completing the changeover to LTE. As a consequence, High Speed Packet Access (HSPA) Evolution is being adopted in parallel with LTE by updating software for existing UMTS infrastructure.

Not only does HSPA Evolution support high-speed throughput technologies such as 64QAM, MIMO, DC-HSDPA (Dual Cell High Speed Downlink Packet Access), and Uplink 16QAM, but it also includes upgraded functions for power consumption, radio resources (CPC), and Enhanced Cell FACH. Anritsu developed the MD8480C as a UMTS base station simulator supporting these HSPA Evolution functions. In addition, it also supports Inter-RAT tests with GSM as well as Lossless Inter-RAT LTE tests when used in conjunction with the MD8430A.

This article explains the MD8480C HSPA Evolution functions and how they have been implemented.

Figure 1 MD8480C Signalling Tester

2 Development Concepts

The development concepts for the MD8480C HSPA Evolution functions are outlined below.

(1) Assured compatibility with existing functions
(2) Upgraded hardware with minimum user costs
(3) High throughput speed (Down: 43.2 Mbps, Up: 11.52 Mbps) with support for Rel. 7 and Rel. 8
(4) Easy updating supporting quarterly revisions of 3GPP standards

3 Hardware System Design

Figure 2 shows the composition of the MD8480C boards.

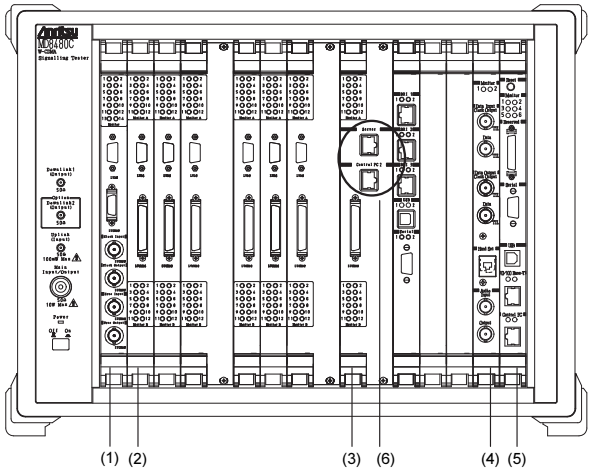

Figure 2 Front Panel of MD8480C

Basically, the standard MD8480C configuration is composed of a power supply unit, RF unit, and the following Digital Control Boards:

(1) Timing Generator
(2) BTS Boards
(3) L2 Board
(4) Voice Codec
(5) CPU Board

To support HSPA Evolution, the RF unit, BTS boards and L2 board have been upgraded from these.

3.1 RF Unit

The RF-function-related HSPA Evolution standards are:

- 5-MHz Signal Bandwidth (10 MHz at DC-HSDPA)
- QPSK, 16QAM, 64QAM Data Modulation Methods
- MIMO, DC-HSDPA

To assure communications quality at 64QAM modulation, we developed a new signal generator (SG) unit with upgraded Downlink signal quality.

3.2 BTS and L2 Boards

The BTS board performs Layer-1 (Physical layer) processing and the L2 board performs Layer-2 (MAC/RLC) processing.

The Downlink and Uplink maximum throughputs have been extended as follows in accordance with the Rel. 7 and 8 standards.

<MIMO, DC-HSDPA>

14.4 Mbps → 43.2 Mbps

<Uplink 16QAM>

5.76 Mbps → 11.52 Mbps

The BTS and L2 boards require more than twice the previous processing capacity. Since neither the BTS boards nor the L2 board have the memory, communication speed or processing speed to support this higher-speed processing, they have been partly replaced by a large capacity FPGA with lower power consumption. Moreover, as well as adding a built-in 10/100M Ethernet port to the CPU board, a Gigabit Ethernet port has been added to the L2 board (Figure 2 (6)).

4 Software System Design

4.1 Software Blocks

Figure 3 shows the MD8480C software configuration. Users create scenarios executing predefined operations. Next, the scenarios are executed by the GUI on the PC controller. At scenario execution, the procedure described in the scenario is executed; control for each layer and L3 signalling messages are sent and received by exchanging messages called primitives between each protocol.

Each processing section of the MD8480C main frame sends and receives data in accordance with received primitives to control the hardware.

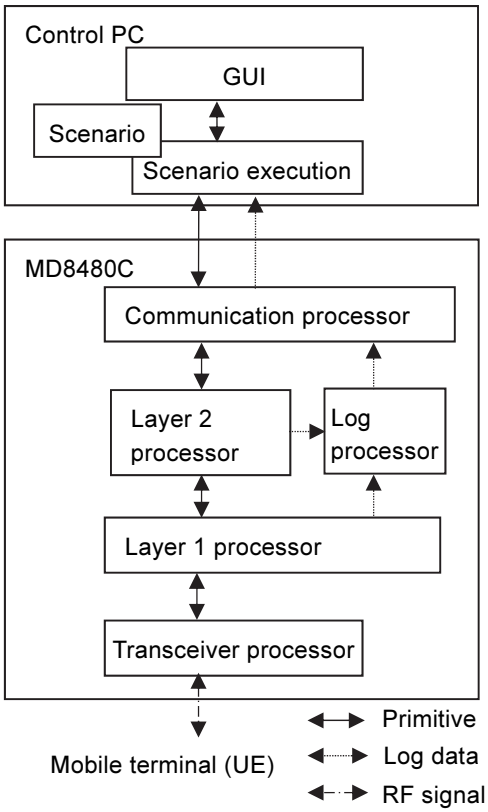

Figure 3 Software Block Diagram

4.2 Reducing PCI Communications Time

Figure 4 shows the MD8480C internal data communications bus configuration. Communications between boards as well as communications between onboard DSP are executed using the PCI bus, but supporting high-speed throughput increases the communications time, making the PCI bus speed inadequate. Consequently, part of the PCI communications has been replaced by the FPGA to solve the problem of concurrent processing with PCI communications. Access to the data server is handled by the communications processing, but adding the Gigabit Ethernet port to the L2 board and using direct access from the L2 board has increased data throughout and reduced communications time.

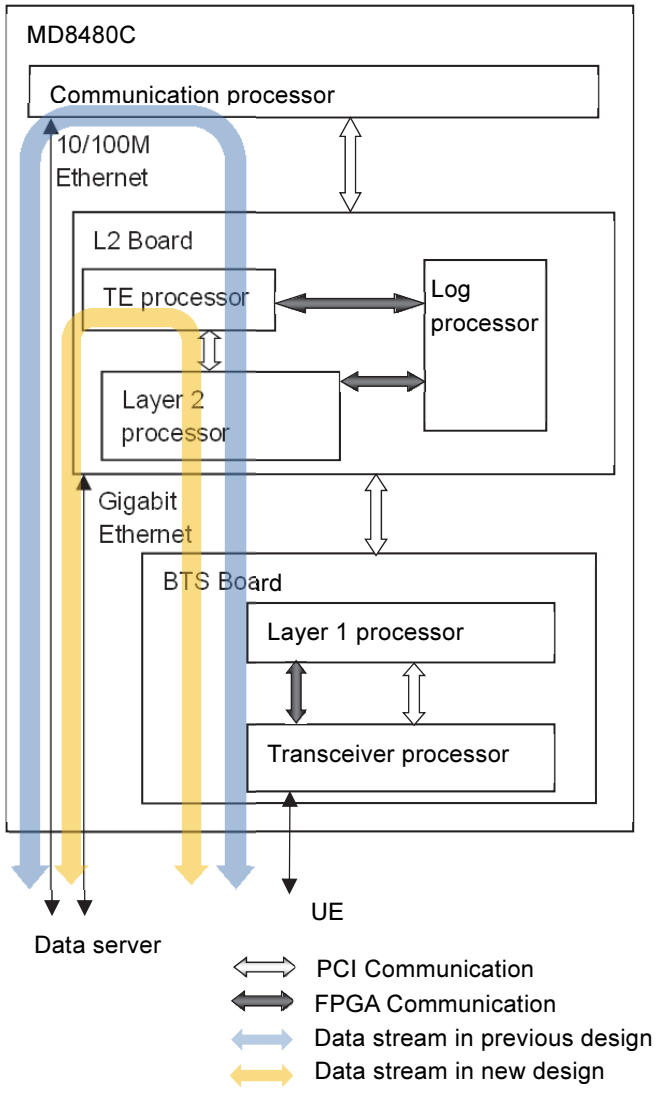

Figure 4 MD8480C Communication Configuration

5 Added and Revised Functions

5.1 GUI and WNS Evolution

5.1.1 Control Software

The MD8480C is controlled by application control software running on an external PC. The control software sets connections with the digital IQ output, RF unit, etc., using the screen shown in Figure 5 and performs settings such as the Physical channel power and channelization code, timing, etc. Settings for new connection paths like MIMO and DC-HSDPA have been added while still retaining the previous familiar MD8480C user operability. In addition, the measurement functions also support unique parameters for MIMO and DC-HSDPA.

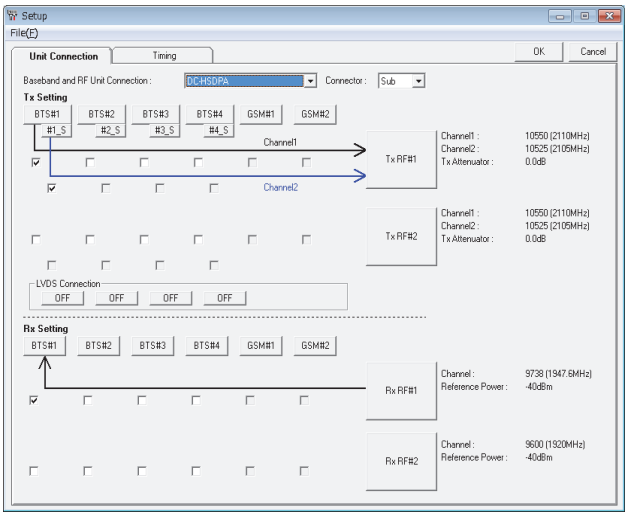

Figure 5 Control Software Setup Window (DC-HSDPA)

5.1.2 WNS Evolution

Wireless Network Simulator (WNS) Evolution uses control application software installed on the same PC controller to simulate base station operation using only GUI operations. Creation of scenarios for connection with mobile terminals (UE) requires expert knowledge of each layer, but using WNS Evolution offers a scenario-free test environment for voice, data packet, SMS, Rx Diversity, Fading Environment, Additive White Gaussian Noise (AWGN), Orthogonal Channel Noise Simulator (OCNS), etc., tests using simple operation screens on the PC controller. Data packet communications tests are also supported by HSPA Evolution using 64QAM, DC-HSDPA, and CPC functions.

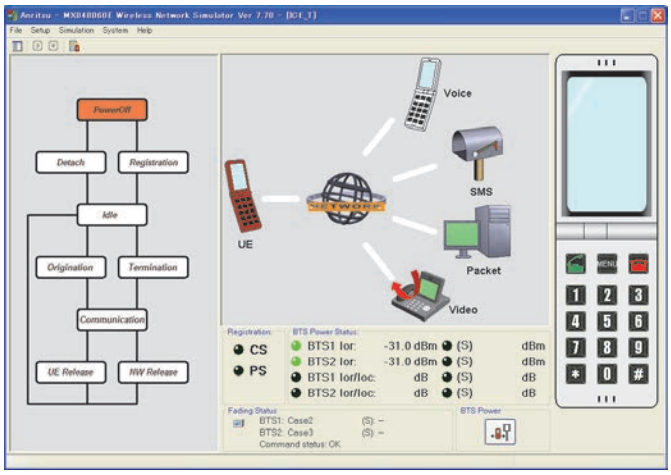

Figure 6 WNS Evolution Window

5.2 MIMO and DC-HSDPA

MIMO and DC-HSDPA increase data throughput by more than twice the previous HS-DSCH data speeds as shown in Figure 7. Consequently, two data encoding processings are now required.

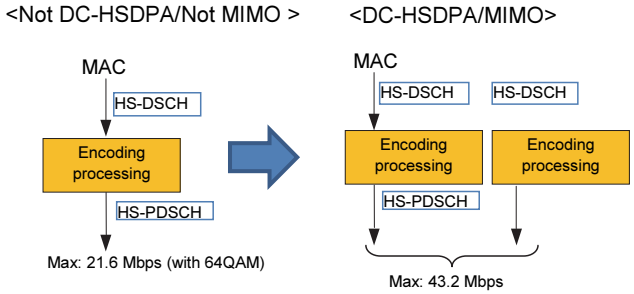

Figure 7 Layer-1 Coding

Previous encoding processing was handled by DSP with the FPGA performing modulation. However, the DSP processing speed and memory are inadequate for performing two encoding processings, so encoding has been moved to the FPGA to achieve high-speed throughput processing and reduced latency (Figure 8).

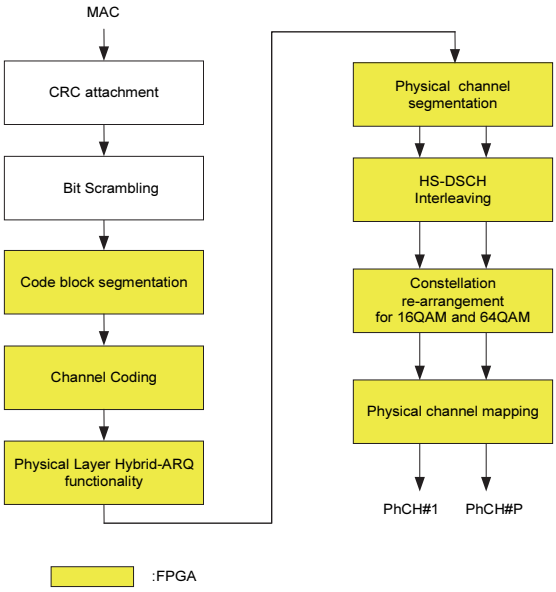

Figure 8 Details of Layer-1 Encoding

5.3 Uplink 16QAM

The following Rx functions have been added to support high-speed throughput:

(1) High-order modulation technologies (16QAM)

(2) Power Boost Mode

Support for 16QAM (uses I and Q phases with 4PAM) has been added to the previously supported BPSK and QPSK (uses I and Q phases with BPSK) technologies.

Because the processing time was insufficient to receive 16QAM signals at the previous processing speed, we speeded-up the processing. The previous Rx processing used the FPGA near the input section for despread and normalization, etc., with decoding performed by the DSP, but part of the decoding has been moved to the FPGA to shorten the processing time and achieve faster speeds (Figure 9).

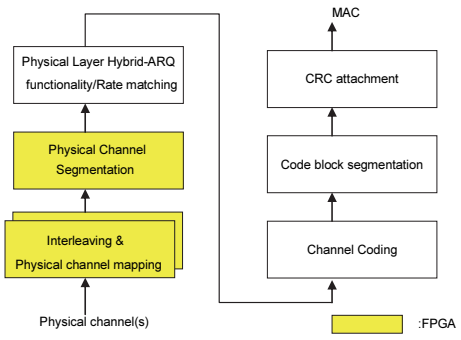

Figure 9 E-DCH Decoding Processing

Item (2) is intended to improve synchronization tracking by supporting the Power Boost mode for combining pilot and data signals with large level differences. Previous synchronization tracking only used the pilot signal (Uplink DPCCH) but when using the Power Boost mode, the timing performance can be degraded due to the relatively small power level of the pilot signal. To solve this problem, in addition to using the pilot signal, we have upgraded the tracking performance by using synchronization tracking using the E-DPCCH to increase the Rx performance.

Due to the above-described improved Rx performance, the accurate reception at Uplink 16QAM, and Power Boost more than doubles (11.52 Mbps) the throughput for HSUPA (High Speed Uplink Packet Access) compared to previous methods.

5.4 Enhanced Log Function

In accordance with the increased throughput of HSPA Evolution, since it has become very difficult to analyze and display the primitive trace records (Trace data) in real time, a function for capturing Trace data requested by the user is now supported.

When this function is triggered, Trace data before and after the trigger are output to a Trace log file (*.log).

As an example, Figure 10 shows output of trace data for a specified range to the Trace log file (*.log) based on the PHY_CRCERR_IND Trace data.

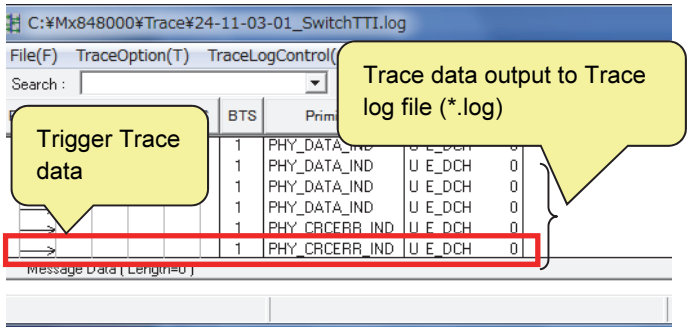

Figure 10 Enhanced Log Function

5.5 Fading Environment Test

The MD8480C supports 3GPP-defined multi-path fading propagation condition tests by using an Anritsu MF6900A as an external fading simulator.

The LVDS connector on the front panel of the MD8480C is connected to the LVDS connector on the back panel of the MF6900A using a dedicated cable to support communications between each BTS board of the MD8480C and the MF6900A. One MD8480C and one MF6900A can support fading environment tests for signals of up to four BTS boards.

The digital baseband signal generated by each baseband board in the MD8480C is transferred to the MF6900A and then returned to the same BTS board after computing the propagation condition model for each carrier (channel #1 and #2 in Figure 11). Subsequently, this digital baseband signal is output from the RF unit after addition of AWGN.

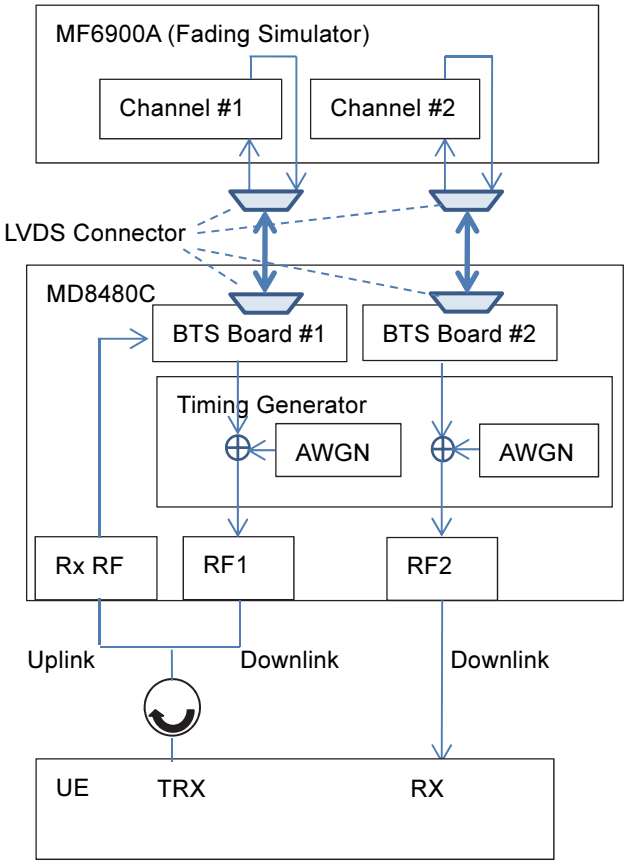

Figure 11 Connection example of the Fading Environment Examination (Rx Diversity Examination)

At DC-HSDPA, one BTS board outputs baseband signals for two carriers. Consequently, we changed the method of transferring digital baseband signals for two carriers to the MF6900A.

The previous digital baseband signal for each carrier transferred the I and Q phases independently for the clock and data pair (total of four for two data signals and two clock signals) but was changed by bundling the I and Q phases so as to change one signal previously used as a clock to data to provide three data signals and one clock signal. Additionally, the headers for synchronizing the three data signal lines were lumped together as one giving better data

transfer efficiency. Changing the transmission methods like this doubled transfer capacity without changing the transmission speed or number of lines.

The above-described change in the transmission method is due to the improved hardware characteristics, such as isometric wiring, and signal waveforms from the front connector to FPGA at upgrade of the BTS board, permitting transmissions supporting digital baseband signals for two carriers.

Furthermore, the digital baseband signal for two carriers sent from one BTS board to the MF6900A is returned to the same BTS board after computing the propagation condition model for each carrier and is then output from the RF unit after AWGN addition.

These modifications made it possible to support a fading test environment even for DC-HSDPA. Moreover, a fading environment can even be configured for Tx Diversity tests requiring multiple antennas by using two BTS boards.

6 Summary

The MD8480C has been upgraded to support development of chipsets and protocols for HSPA Evolution mobile markets.

The evolving support for W-CDMA first, then HSPA, and now HSPA Evolution make the MD8480C an indispensable tool for chipset and mobile terminal vendors validating UMTS technologies worldwide.

It can also be used as a key component in configuring conformance and carrier acceptance inspection test systems for assuring improved UMTS service quality.

Anritsu has developed the MD8480C as a key measurement solution for verification of evolving new UMTS technologies.

References

1) S. Arai, K. Kameda, T. Kamisawa, K. Fukazawa, “移動体通信端末試験装置及び移動体通信端末試験方法”, Patent Application 2012-142670 (2012.7)

2) S. Arai, K. Kameda, T. Kamisawa, K. Fukazawa, “移動体通信端末試験装置及び移動体通信端末試験方法”, Patent Application 2012-142671 (2012.7)

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