Development of Transport Test Platform Supporting Multiple Communication Protocols

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[Summary] The recent spread of smartphones and the resultant explosion in mobile data is increasing the amount of IP packet traffic. On the other hand, Optical Transport Networks (OTN) are being used increasingly for core networks due to their characteristics of high reliability and wide bandwidth. In addition to IP traffic over OTN, there is increasing demand for expandable functions to handle different communications efficiently and for wider bandwidths. We developed the MT1110A Network Master Pro and MT1100A Network Master Flex against this backdrop to meet the increasing need for testers to evaluate optical networks using various communications protocols.

1 Introduction

As part of the trend towards conversion of optical communications networks to full IP, OTN is being adopted to assure integration with existing networks and make effective use of current infrastructure[1]. Furthermore, as the mobile backhaul market converts rapidly to wider bandwidth to cope with explosive increases in mobile data traffic, core and metro networks are deploying new technologies, such as 100GbE, 100G OTN, etc., at a rapid pitch[2].

Against this backdrop, the optical network installation and maintenance (I&M) field increasingly needs a transport network tester for evaluating transport equipment supporting the various communications protocols. In addition, high-bit-rate networks demand both especially high reliability due to the large data volumes and client numbers; reliable evaluation of equipment and networks is a key need at every stage from R&D to manufacturing, deployment and maintenance[3) to 6)].

We have developed the MT1000A Network Master Pro and MT1100A Network Master Flex as compact, lightweight, battery-operated, all-in-one testers to meet the need for instruments to evaluate systems using various communications standards. The all-in-one MT1000A can be used to evaluate equipment and networks using various communications standards at bit rates from 1.5 Mbps to 10 Gbps. Its compact size and battery operation make it the ideal tester for telecoms I&M fieldwork. The all-in-one MT1100A supports the latest network technologies at bit rates from 1.5 Mbps to 100 Gbps to support transport tests in communications network R&D, equipment manufacturing, network I&M, etc. With four ports each supporting 1 Gbps, it can generate and analyze 100G client signals for future 400G networks and incorporates a large number of protocols ranging from existing networks such as SDH/SONET/PDH/DSn, Ethernet, Fibre Channel (FC), and OTN to new technologies. For OTN, these protocols can be mapped as client signals that can be measured and evaluated in detail. Supporting various protocols and mappings requires multiple configuration files for the built-in, large-scale Field Programmable Gate Array (FPGA). Sharing these source codes has improved the development efficiency and maintainability.

2 Development Concept

The development concept was twofold:

(1) Support testing for R&D, manufacturing, and I&M for various networks and transport equipment used by markets ranging from mobile fronthaul to core networks;

(2) Offer an easy-to-use platform for everyone flexibly supporting the needs of each market with a single tester.

Achieving these goals required designing a platform with (a) easy expandability for adding functions, (b) easy operation with no reliance on operator skills, and (c) support for each communication protocol.

2.1 High-Expandability Platform

As well as expandability, portability is a key point for the MT1000A target I&M market. To achieve both expandability and portability, the controller and measurement sections were divided into modules and the measurement section was configured as a swappable attachment. By using this design, new modules for future measurements can be added and existing measurement modules can be used with the controller.

On the other hand, for the MT1100A target markets of R&D and manufacturing, a stackable design was used for the

measurement section, offering an easy way to increase the number of measurement ports in line with the customer's development environment. In addition, the design incorporates expandability up to a maximum of four 100G ports in consideration of future 400G measurement requirements.

2.2 Easy Usability

Achieving the MT1000A and MT1100A key features of functional versatility and expandability ran a risk of reduced operability due to the increase in the number of settings and measurement items. Implementing both multifunctionality and easy operation simultaneously requires efficient layout of required information on screens which was achieved by dividing the application software according to each protocol and evaluation item. So as not to lose the coherent operability feeling, we defined and designed a GUI conceptual model based on an application selector for starting applications, a results file browser for displaying saved test results, a settings screen for setting interface parameters for connecting with the DUT, a test screen for setting test parameters, such as test time, and a results screen for displaying results; this GUI offers coherent operability across all applications.

2.3 Large-Scale FPGA Development Effect and Increased Maintainability

The MT1000A and MT1100A use an FPGA to support a variety of protocols and complex OTN mappings. When using a large-scale FPGA to support a large number of mappings, it is impossible to save all the functions in a single configuration file due to the limited capacity of the FPGA, so the functions were divided between multiple configuration files. A shared source code design was used for all configuration files to achieve good efficiency and maintainability. The required mapping is configured by calling parameters within this source code to enable only the required circuits.

3 Equipment Configuration

3.1 MT1000A Network Master Pro

The MT1000A has a high-visibility, 9-inch LCD touch panel providing optimum operability for each measurement application. Each function is executed by touch-panel operation and the power button is the only 'physical' button—a design that offers compact size and a large screen. Battery powered operation for up to 6 hours is provided in consideration of the need for portability. Measurement modules are mounted in the back panel of the MT1000A and we have developed the MU100010A 10G Multirate Module as the first stage in configuring a measurement system using a combination of measurement modules. The MU100010A has SFP/SFP+, RJ45, BNC, RJ48, and Bantam interface connectors covering a range of bit rates from 1.5 Mbps to 10 Gbps. There are two Rx and Tx ports for all measurement interfaces and each port operates independently. Figures 1 and 2 show the external views of the MT1000A.

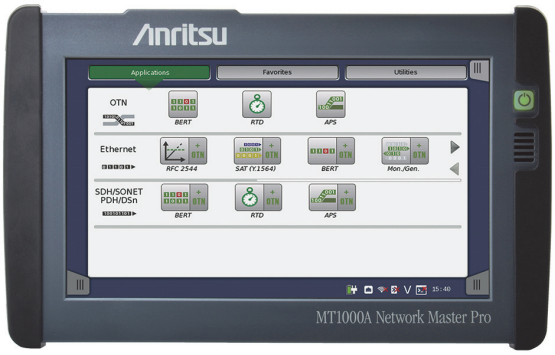

Figure 1 MT1000A Front Panel

257 (W) × 164 (H) × 77 (D) mm

Figure 2 MT1000A/MU100010A Interface Panel

3.2 MT1100A Network Master Flex

With a 12-inch touch-panel LCD, the MT1100A shares the same GUI as the MT1000A for fully compatible operability. Up to two measurement modules can be mounted between the MT1100A main unit and power module. There are two power modules—the MU110001A Battery/AC Power Module for portable operation, and the MU110002A AC Large-Capacity Power Module used mainly for bench-top operation. Three measurement modules have been developed: the MU110010A 10G Multirate Module, the MU110011A 100G Multirate Module, and the MU110012A 40G/100G Module CFP2. The MU100010A for the MT1000A shares the same hardware as the MU110010A for the MT1100A; the former has SFP/SFP+, RJ45, BNC, and RJ48 measurement interfaces covering bit rates from 1.5 Mbps to 10 Gbps, while the latter has CFP, QSFP+, SFP/SFP+, and RJ45 measure-

ment interfaces covering bit rates from 10 Mbps to 100 Gbps. The MU110012A has two ports for each of the CFP2, CXP, and QSFP+ measurement interfaces for higher-density coverage from 40 Gbps to 100 Gbps. Figures 3, 4, 5, and 6 show the external views of these modules.

Figure 3 MT1100A External View

320 (W) × 225 (H) × 188 (D) mm
(with MT1100A + MU110011A + MU110001A)

Figure 4 MU110010A Interface Panel

Figure 5 MU110011A Interface Panel

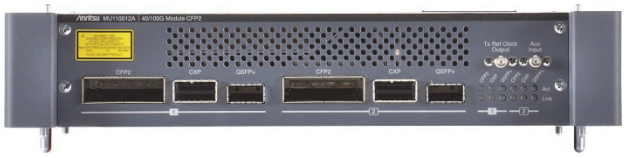

Figure 6 MU110012A Interface Panel

4 Design Strategy

4.1 MT1100A Stackable Configuration

The I&M market requires compact portability whereas the R&D and manufacturing markets require multiple modules. Trying to support multiple modules using the previous slot-type main-frame design cannot support the I&M market's requirements for compactness. Consequently, the MT1100A uses a stacking design in which connectors on both sides of each measurement module connect to other modules. Figure 7 shows the communications and control signals, and the power line to each module. By using this type of configuration, the user can select any combination and number of modules meeting the application requirements.

In addition, to simplify installation, reduce the parts count and cut costs, configuration files for the FPGA, etc., are saved at the controller side to configure the FPGA for the measurement module from the controller side. Moreover, chaining via the FPGA is used to achieve a future-proof design with assured expandability and no restrictions on the number of installed modules while securing good signal quality on the communications bus. Further, software access addresses are allocated by writing to the FPGA register of the measurement module.

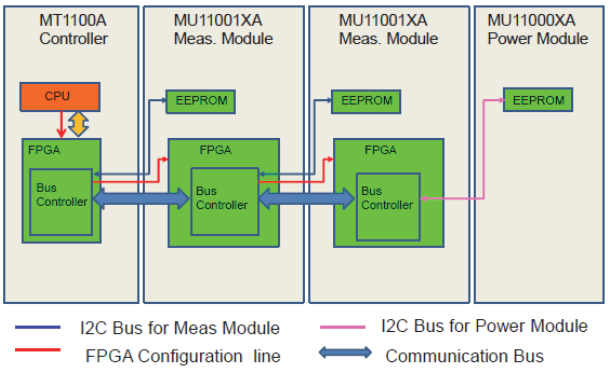

Figure 7 Stackable Configuration Connection Diagram

The actual implementation method is explained here. The signal lines for the EEPROM storing information about the measurement module and FPGA configuration are connected to the module immediately upstream. After powering-up, the MT1100A reads the module information from the EEPROM of the first measurement module and configures the FPGA. As a result, communications between the controller module, first module, and FPGA become enabled. The address of the first module is written to the register of this FPGA. Next, the EEPROM of the second module is read via the FPGA of the first measurement module, the FPGA of the second module is configured via the FPGA of the first module, and the address of the second module is written.

Using this method makes it possible to increase the number of modules that can be installed in the future. Additionally, the stackable design is used because unlike development of new modules for previous slot-type main frames, there is no problem with module size dependency on slot size. Similarly, limits on the thickness of each meas-

urement module disappear, supporting flexible development of future additional measurement modules.

4.2 Easy-to-Use GUI

We defined a conceptual model to assure coherent operability between all MT1000A and MT1100A measurement applications. This conceptual model has two functional levels—the desktop, and the workspace.

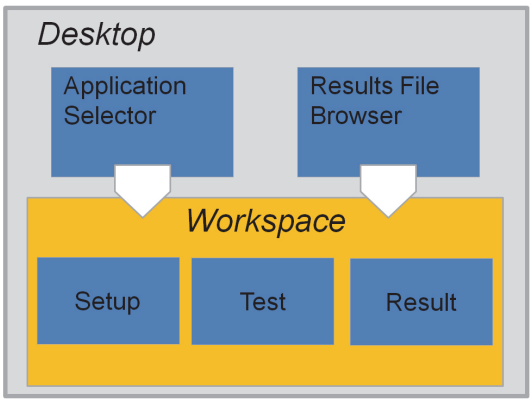

Figure 8 GUI Outline

The desktop is the entry level displayed immediately after powering-up. It is composed of the Application Selector for starting new applications, the Results File Browser for displaying saved test results, and the Workspace.

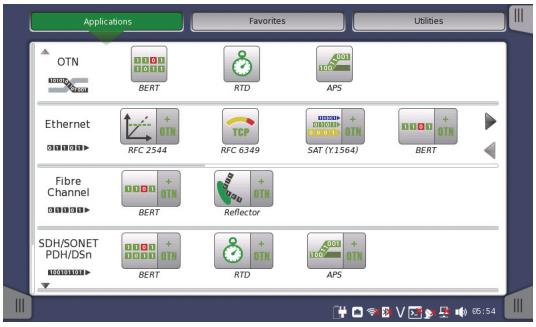

Figure 9 Application Selector Screen

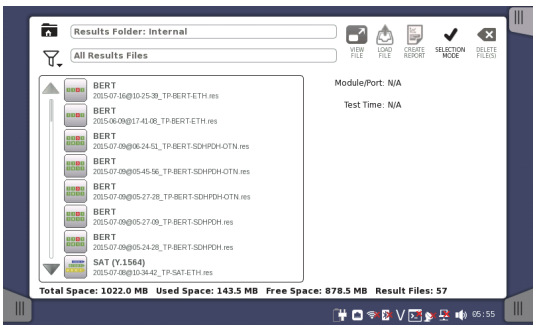

Figure 10 Results File Browser Screen

The Workspace accommodates running applications and is itself composed of three fields: 1. [Settings] for setting interface parameters for connecting with the DUT, 2. [Test] for setting test condition parameters, such as test time, and 3. [Results] for displaying measurement results.

Scrolling between the desktop and workspace fields is done using tabs displayed at the screen top, bottom, left and right.

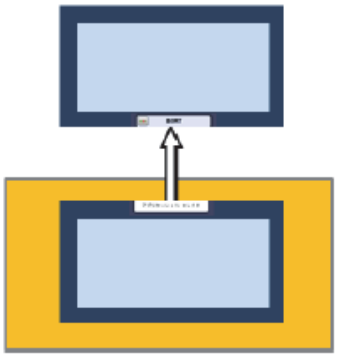

Figure 11 Screen Scrolling (Up/Down) at Desktop

Figure 12 Screen Scrolling (Left/Right) at Desktop

In addition to these tab operations, touching the Settings, Test, and Results labels, which are always displayed at the screen bottom, scrolls the screen horizontally.

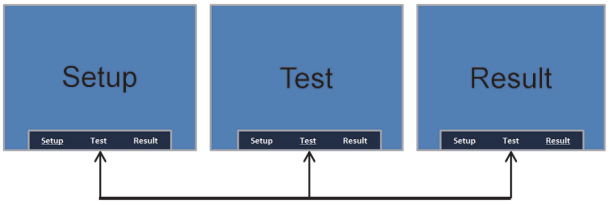

Figure 13 Sub-screen Scrolling at Workspace

The software frameworks for implementing this screen hierarchy are provided as a shared library. Application developers can use the shared framework Application Program Interface (API) to register more customized application screens within the Settings, Test, and Results screens. As a result, application developers can both edit the functional design of applications as well as add new applications without losing operational coherence between applications.

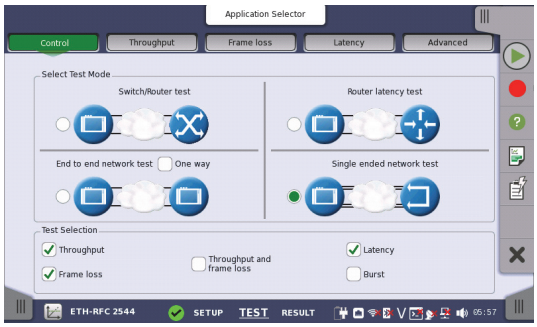

Figure 14 Workspace (RFC 2544 Setting Screen)

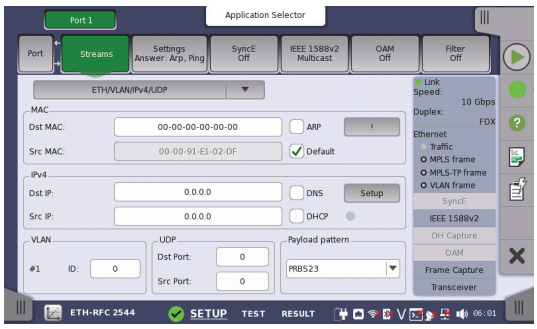

Figure 15 Workspace Example (RFC 2544 Test Screen)

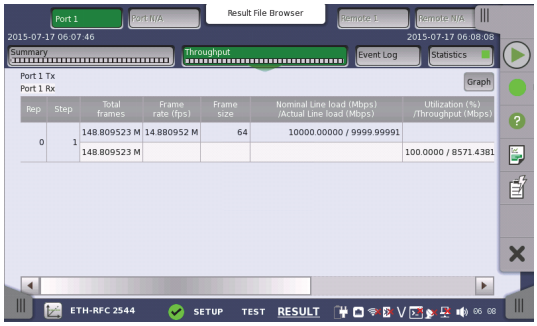

Figure 16 Workspace Example (RFC 2544 Results Screen)

Frameworks were implemented using object oriented design and the details of the conceptual model are concealed in the API base class providing the framework. Not only can application developers implement sub-classes inheriting this base class, they do not need to be conscious of the conceptual model at all. This programming method assures both expandability through addition of various new applications, and operational coherency of the MT1000A and MT1100A.

4.3 Support for Complex Networks

4.3.1 OTN Mappings

Signals and protocols are being developed and deployed to optimize communications in various fields. In addition, configurations for assuring compatibility between protocols and supporting long-distance transmissions are being investigated. Conventional communications technologies also continue to be used while developing and deploying new protocols. More recently, complex networks are being configured sharing both evolving new and old protocols side-by-side. As shown in Figure 17, optimized communications and protocols are being deployed in various fields such as TDM, SAN, mobile backhaul, etc., and new R&D is being made into configurations supporting compatibility between these protocols and long-distance transmissions. Today's networks are continuing to evolve like this through complex sharing of these new and old protocols.

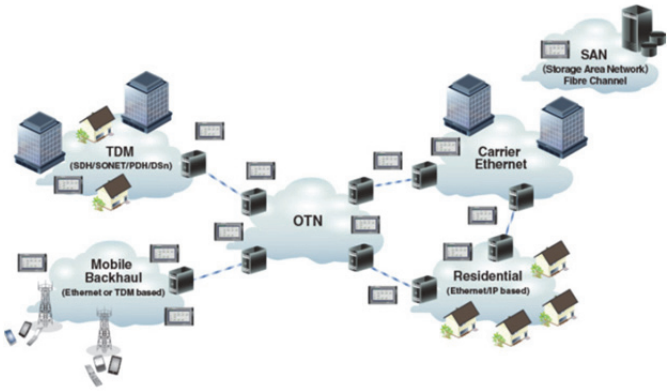

Figure 17 Relationships between Protocols and MT1000A/MT1100A

The MT1000A and MT1100A support evaluation of Ethernet now being used in many fields, Fibre Channel (FC) used in storage networks, SDH/SONET/PDH/DSn legacy technologies used by core and access networks, and the various OTN technologies used on core networks to assure high-quality long-distance transmissions. OTN supports mapping of Ethernet, FC, SDH/SONET, and pseudo-random pattern signals as client signals, and the MT1000A and MT1100A have generating and measureing functions same as Ethernet, FC, and SDH/SONET application. As a result, these testers can supply near-to-live OTN signals to the DUT, as well as perform detailed analyses of mapped client signals. Figure 17 shows the OTU4 mappings supported by the MU110011A/MU110012A.

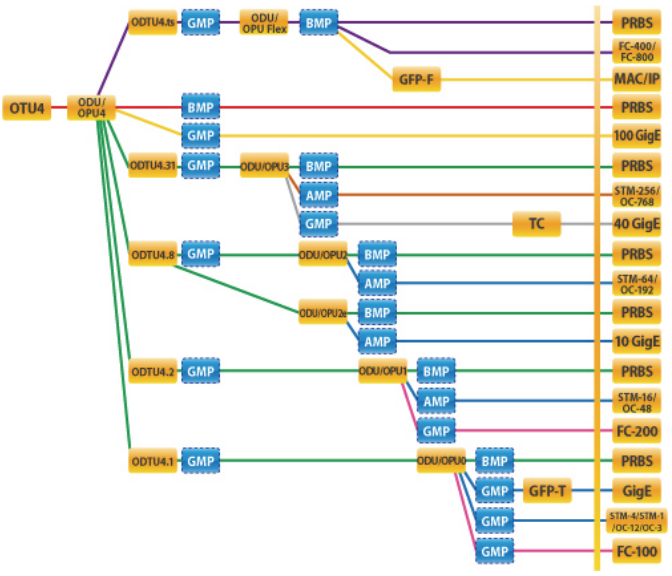

Figure 18 OTU4 Mappings

4.3.2 Improved FPGA Usage Efficiency and Maintainability

The OTN standard defines various technologies, such as OTU1, OTU2, OTU3, OTU4, etc., each of which uses the above-described mappings (multiplexings). Using the MU110011A and MU110012A incorporating a large-scale FPGA supports generation and Rx analyses of these OTN-recommended mappings. When using a large-scale FPGA to support many mapping configurations, limitations on the FPGA storage make it impossible to save all the functions in one FPGA configuration file. Consequently, we have provided a configuration file for each mapping that is overwritten according to the screen settings. There are more than 40 required configuration files, requiring a lot of time and difficult maintenance to provide support for each separate source code.

To achieve more efficient design and maintenance, common source code was used for all configuration files; the mappings are configured by setting parameters in this source code to enable only the required circuits. Since the OTN frame format is the same whatever the bit rate, implementing the OTN mappings by sharing source code makes it possible to share the data stream bit width and optimize the error insertion circuits, etc. In practical terms, eliminating the need to provide source code for every mapping improves the FPGA usage efficiency and maintainability.

4.3.3 Connecting FPGAs using Fast Wideband Interface

The MU110011A and MU110012A can both map Ethernet signal with full test functions as client signal onto OTU4 and OTU3 frame. This is implemented by incorporating two FPGAs in one measurement module; one FPGA is used for OTU framing/deframing, while the other is used for generating and analyzing the client signals. Using the Interlaken protocol assures a bandwidth of better than 103 Gbps between the two FPGAs for easy data exchange[7]. As shown in Figure 19, there is a risk of skew generation in the signal line between the two FPGAs but the phase is maintained by Deskewing using the above-described protocol. A gearbox adjusts the clock synchronization and bit width.

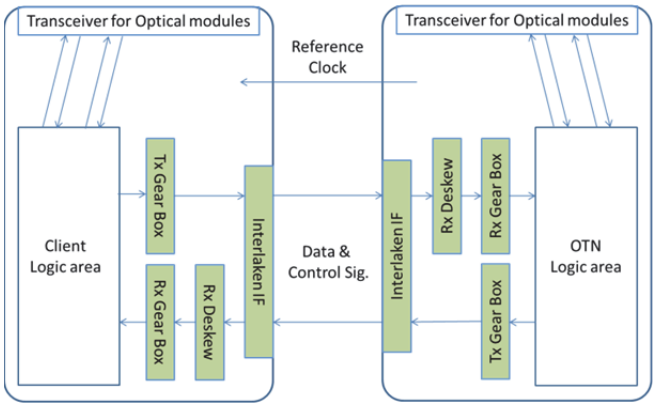

Figure 19 Inter-FPGA High-Speed Interface Block Diagram

4.3.4 Supporting Various Applications using Partial Reconfiguration

As described above, the MT1000A and MT1100A support a variety of communications signals and protocols. In addition, the multiple measurement ports can be used independently because the testers are designed so that switching applications and stopping/starting measurement has no effect between ports.

We used the partial reconfiguration technology to implement this design. This technology divides the FPGA into several internal areas each of which can be configured just by specifying the required FPGA configuration file. Conventionally, control of all ports had to be stopped momentarily at application switching, etc., because it was necessary to configure all areas of the FPGA, even when supporting multiple ports provisionally.

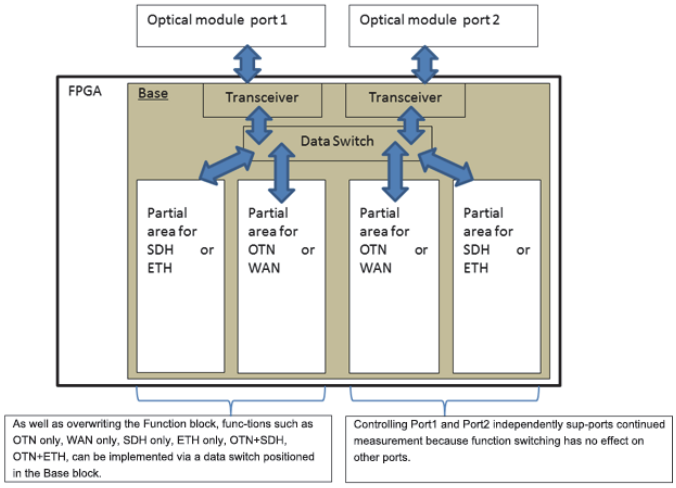

Figure 20 MU100010A/MU110010A Partial Area Allocations

Figure 20 shows the partial areas for the MU100010A and MU110010A allocated by this developed partial configuration function. The FPGA is divided into a Base area plus four partial areas; two partial areas are allocated to each port. The Base area is written to once and cannot be overwritten again until the power is cut. It is composed of interfaces with the CPU, high-speed transceiver blocks, various I/O pins, a data switch, interfaces with external devices, control block, etc. On the other hand, it is possible to achieve a design with a high degree of freedom and circuit arrangement by specifying and following the rules for the connection method between the partial areas and base area as well as the allocation of resources within the FPGA. Moreover, the partial area source code is shared to support applications with functional differences between multiple ports, as well as excellent development efficiency and maintainability.

Using this partial configuration makes it possible to make settings and switch applications at one port with no effect on other ports, and makes it easy to support DUT insertion testing and signal monitoring, etc., in the passthrough mode.

5 Summary

The recent explosive growth of mobile data traffic resulting from the spread of smartphones, tablets, etc., is driving 'All IP' conversion of Core Network, integration of existing networks, and the spread of OTN offering high reliability. Against this backdrop, there is increasing need for a transport network tester to evaluate transmission equipment and networks using the various communications methods and bit rates. To meet this need, we have developed the all-in-one, compact, battery-operated MT1000A for evaluation of signal protocols at I&M, supporting bit rates from 1.5 Mbps to 10 Gbps. Its new sister tester is the MT1100A designed for network I&M as well as development and manufacturing of network equipment supporting bit rates from 1.5 Mbps to 100 Gbps.

Both platforms are composed of hardware and software with excellent expandability to support deployment of future higher-speed and complex optical networks by offering easy-to-use and accurate measurement applications increasing the quality of optical network evaluation.

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